TEST NUMBER 1

Generics values:

|  |  |  |
| --- | --- | --- |
| Comments | Value | Name |
|  | 1 | reset\_polarity\_g |
|  | 1 | enable\_polarity\_g |
| Each the number og addresses is RAM in | 3 | signal\_ram\_depth\_g |
| "word" width – line in the RAM | 8 | signal\_ram\_width\_g |
| The number of recorded signals is | 4 | record\_depth\_g |
| BUS width of the information entering the component | 8 | data\_width\_g |
| Word width in WB protocol | 8 | Add\_width\_g |
| Number of signals we record in each iteration | 8 | num\_of\_signals\_g |

Variables values:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Comments | Value | | | Name |
| Inputs | | | | |
|  | 50 duty cycle | | | clk |
|  | 120-20000 | | 0-119 | Reset |
| 0 | | 1 |
|  | 220-20000 | | 0-219 | Enable |
| 1 | | 0 |
| Precentage of data recorded after trigger rise | 00000000 | | | Trigger position in |
| rise | 00000000 | | | Trigger type in |
| Counter- 500 time period | 0-39 | | | data\_in |
|  | 3000-20000 | | 0-2999 | trigger |
| 1 | | 0 |
| Come from WB. repeater | 400-500 | | 0-400 | data\_in\_valid |
| 1 | | 0 |
| Come from WB. repeater | 400-500 | | 0-400 | trigger\_in\_valid |
| 1 | | 0 |
| Outputs | | | | |
| When data\_in\_valid and trigger\_in\_valid signals rise at stste send\_out\_data\_and\_addr, data out is been update | Update every 500 ns  (5 clk cycles) | | | Data out of wc |
| When data\_in\_valid and trigger\_in\_valid signals rise at stste send\_out\_data\_and\_addr, addr out is been update | Update every 500 ns  (5 clk cycles) | | | addr\_out\_to\_RAM |
| Rise when we recorded all the data | 11500-20000 | 0-11500 | | write\_controller\_finish |
| 1 | 0 | |
| When trigger is found and all data is recorded, we send out the address of the relevant data in the RAM | 11400-20000 | 0-11400 | | start\_addr\_out |
| 101 | 0 | |
| When trigger is found and all data is recorded, we send out the array row of the relevant data in the RAM | 11400-20000 | 0-11400 | | start\_array\_row\_out |
| 0 | 0 | |
| Length is number of RAMs, to enable the N RAM we put 1 in the N place and all the other is 0 | Enable the correct RAM when we send the data and address out | | | din\_valid |

Explanation:

The trigger type is set to 'rise'. The information will be recorded entirely after trigger rise,meaning from the moment the trigger rises we'll wait 16 recording cycles(each cycle is 5 clk cycles),then we'll extract an address to the next component.

קבענו את סוג הטריגר לעלייה. המידע יוקלט כולו לאחר עליית הטריגר- כלומר מרגע שאות טריגר עולה, נחכה 16 מחזורי הקלטה (כל מחזור הקלטה הוא של 5 מחזורי שעון) ואז נוציא כתובת לרכיב הבא.

מחזור הקלטה-

1. המידע נדגם
2. בדיקה האם התרחשה עליית טריגר
3. שליחת מידע וכתובת רלוונטים לRAM
4. בדיקה האם כל המידע הוקלט
5. במידה ולא הוקלט כל המידע- חישוב הכתובת הבאה.
6. במידה והוקלט כל המידע- חישוב כתובת תחילת המידע הרלוונטי

Recording cycle:

1. The information is being sampled.
2. Check whether there was a trigger rise.
3. Sending relevant information and address to the RAM.
4. Check whether the information was recorded entirely.
5. In case there is missing information- calculate the next address.
6. In case the information has been recorded properly- calculate the start address of the relevant information.

תיאור מערך RAM:

עומק מידע בRAM בודד- 8

עומק מידע שנדרש להקלטה- 16

רוחב RAM בודד- 8

מספר סיגנלים להקלטה- 8

ניתן לראות כי נדרשים שני RAMs על מנת להקליט את כל המידע.

כאשר אנו מאפשרים את הRAM הראשון din\_valid=01, כאשר אנו מאפשרים את הRAM השני din\_valid=10. שניהם עולים למשך מחזור שעון אחד בכל מחזור הקלטה, ובשאר הזמן יהיו 00

Description of the RAM composition:

-information depth of single RAM- 8

-information depth needed for recordind-16

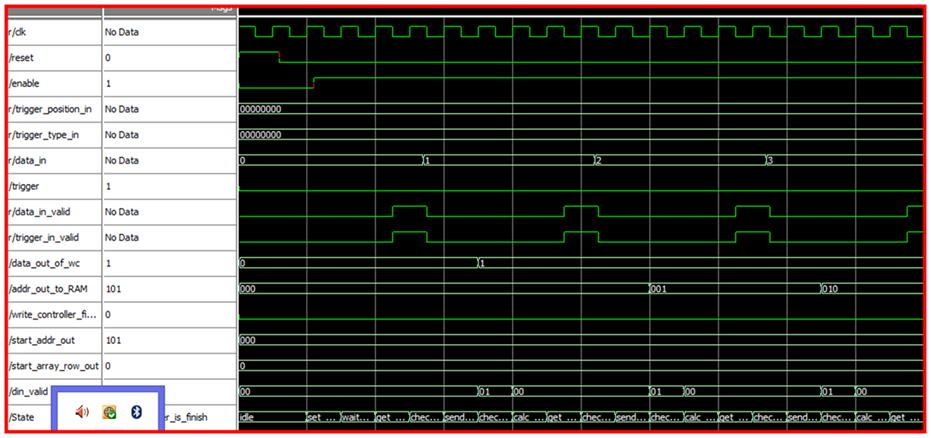
-width of a single RAM-8

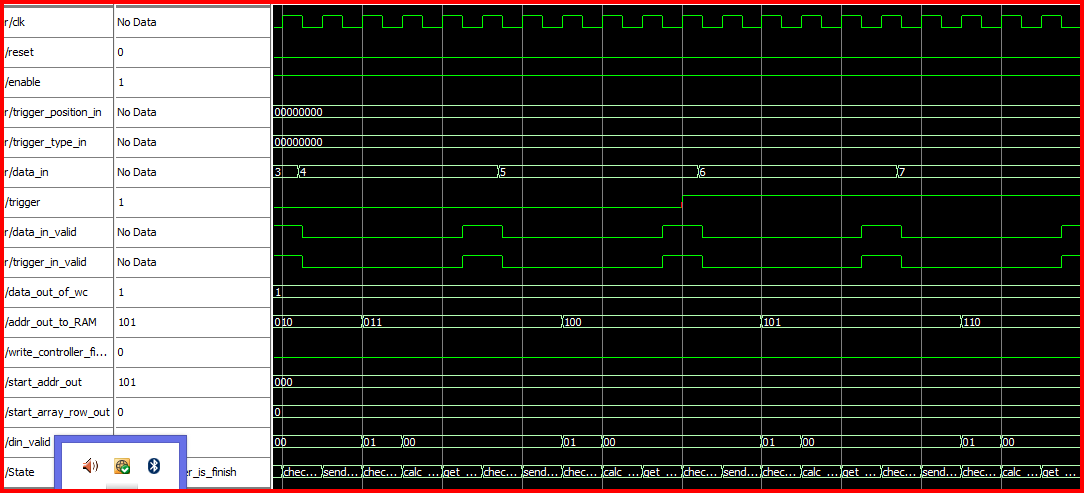
-numbers of signals for recording-8

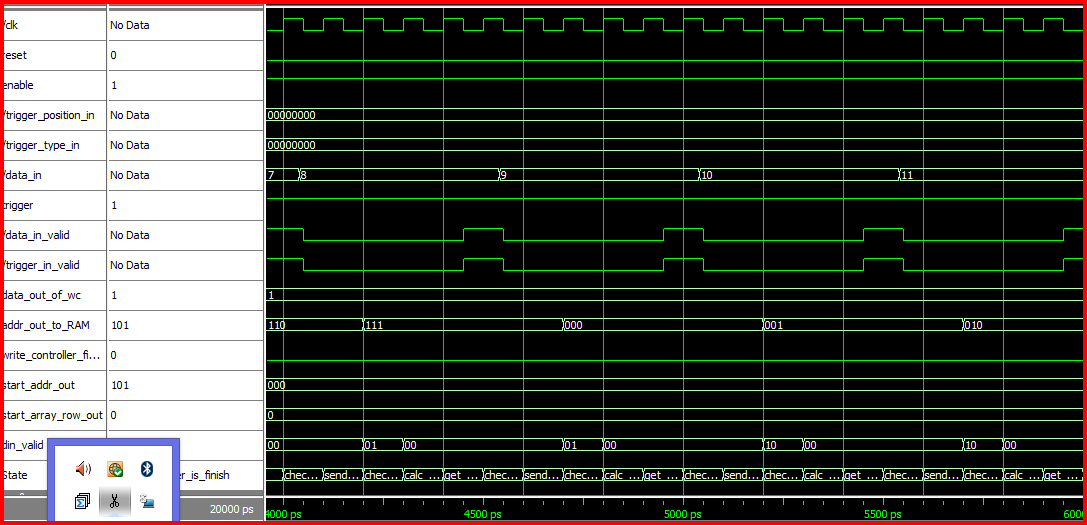
It takes two RAMs to record the entire information.

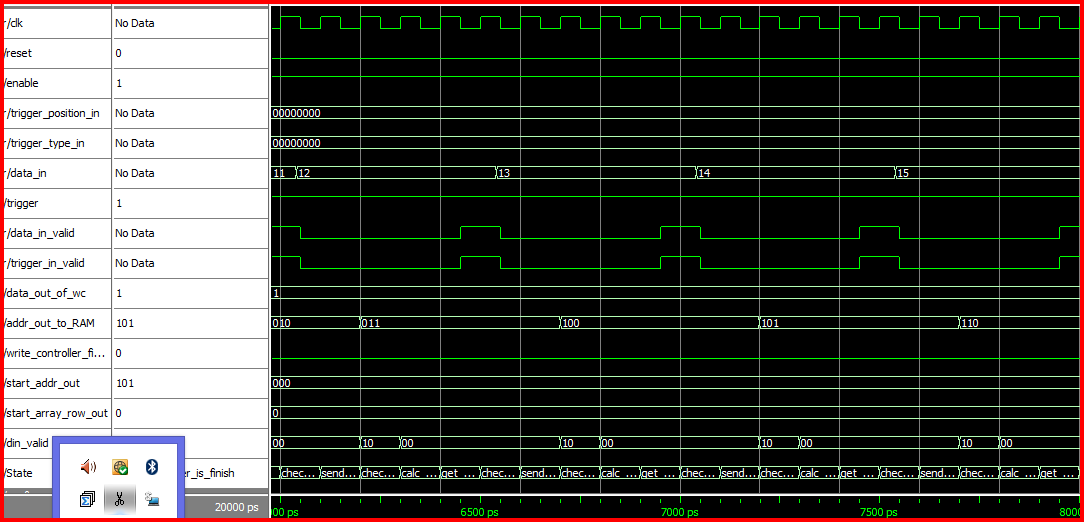
When we enable the first RAM, din\_valid=01, when we enable the second RAM, din\_valid=10. They both rise for one clock cycle in each recording cycle, the rest of the time it will be 00.

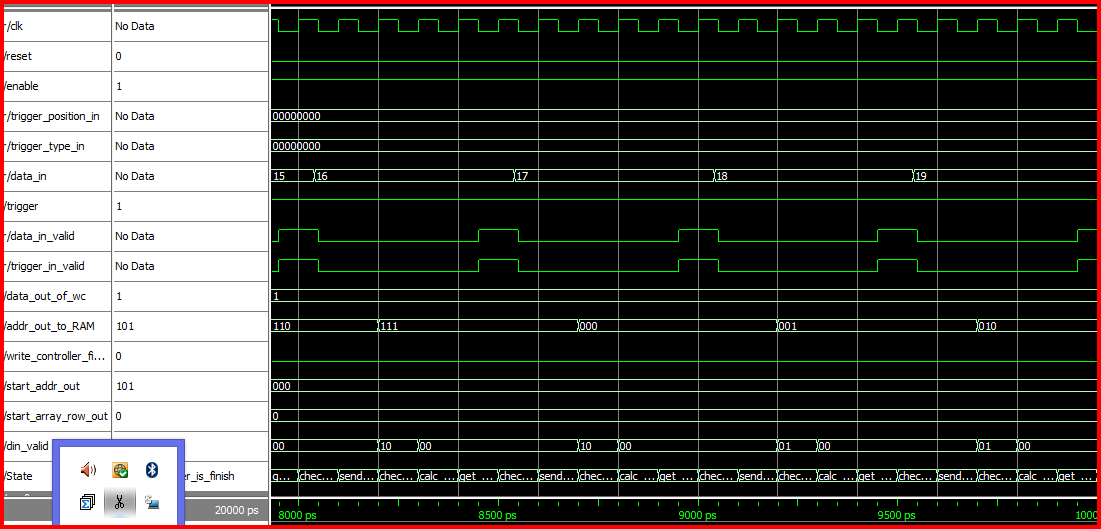
Simulation:

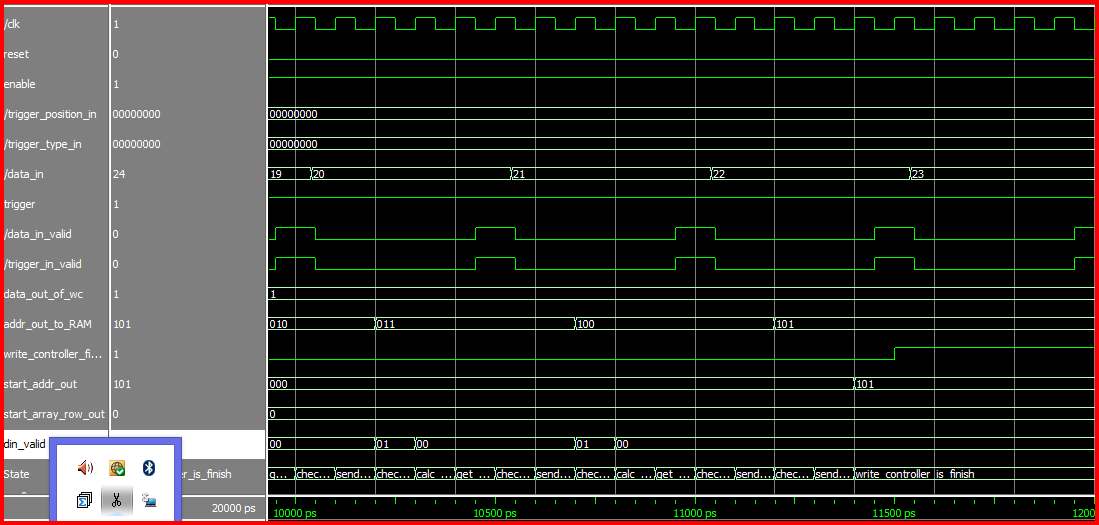












ניתוח:

TEST NUMBER 2

Generics values:

|  |  |  |
| --- | --- | --- |
| Comments | Value | Name |
|  | 1 | reset\_polarity\_g |
|  | 1 | enable\_polarity\_g |
| Each the number og addresses is RAM in | 3 | signal\_ram\_depth\_g |
| "word" width – line in the RAM | 8 | signal\_ram\_width\_g |
| The number of recorded signals is | 4 | record\_depth\_g |
| BUS width of the information entering the component | 8 | data\_width\_g |
| Word width in WB protocol | 8 | Add\_width\_g |
| Number of signals we record in each iteration | 8 | num\_of\_signals\_g |

Variables values:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Comments | Value | | | Name |
| Inputs | | | | |
|  | 50 duty cycle | | | clk |
|  | 120-20000 | | 0-120 | Reset |
| 0 | | 1 |
|  | 220-20000 | | 0-220 | Enable |
| 1 | | 0 |
| 50% | 00110010 | | | Trigger position in |
| One (3 high) | 00000010 | | | Trigger type in |
| Counter- 500 time period | 0-39 | | | data\_in |
|  | 10000-20000 | | 0-10000 | trigger |
| 1 | | 0 |
| Come from WB. repeater | 400-500 | | 0-400 | data\_in\_valid |
| 1 | | 0 |
| Come from WB. repeater | 400-500 | | 0-400 | trigger\_in\_valid |
| 1 | | 0 |
| Outputs | | | | |
| When data\_in\_valid and trigger\_in\_valid signals rise at stste send\_out\_data\_and\_addr, data out is been update | Update every 500 ns  (5 clk cycles) | | | Data out of wc |
| When data\_in\_valid and trigger\_in\_valid signals rise at stste send\_out\_data\_and\_addr, addr out is been update | Update every 500 ns  (5 clk cycles) | | | addr\_out\_to\_RAM |
| Rise when we recorded all the data | 11500-20000 | 0-11500 | | write\_controller\_finish |
| 1 | 0 | |
| When trigger is found and all data is recorded, we send out the address of the relevant data in the RAM | 11400-20000 | 0-11400 | | start\_addr\_out |
| 101 | 0 | |
| When trigger is found and all data is recorded, we send out the array row of the relevant data in the RAM | 11400-20000 | 0-11400 | | start\_array\_row\_out |
| 0 | 0 | |
| Length is number of RAMs, to enable the N RAM we put 1 in the N place and all the other is 0 | Enable the correct RAM when we send the data and address out | | | din\_valid |

Explanation:

The trigger type is set to 'one'. The information will be recorded after trigger will be in high mode for 3 cycles. From the moment that we will find trigger rise we'll wait 8 recording cycles (each cycle is 5 clk cycles), then we'll extract a start address to the next component.

Recording cycle:

1. The information is being sampled.
2. Check whether there was a trigger rise.
3. Sending relevant information and address to the RAM.
4. Check whether the information was recorded entirely.
5. In case there is missing information- calculate the next address.
6. In case the information has been recorded properly- calculate the start address of the relevant information.

Description of the RAM composition:

-information depth of single RAM- 8

-information depth needed for recordind-16

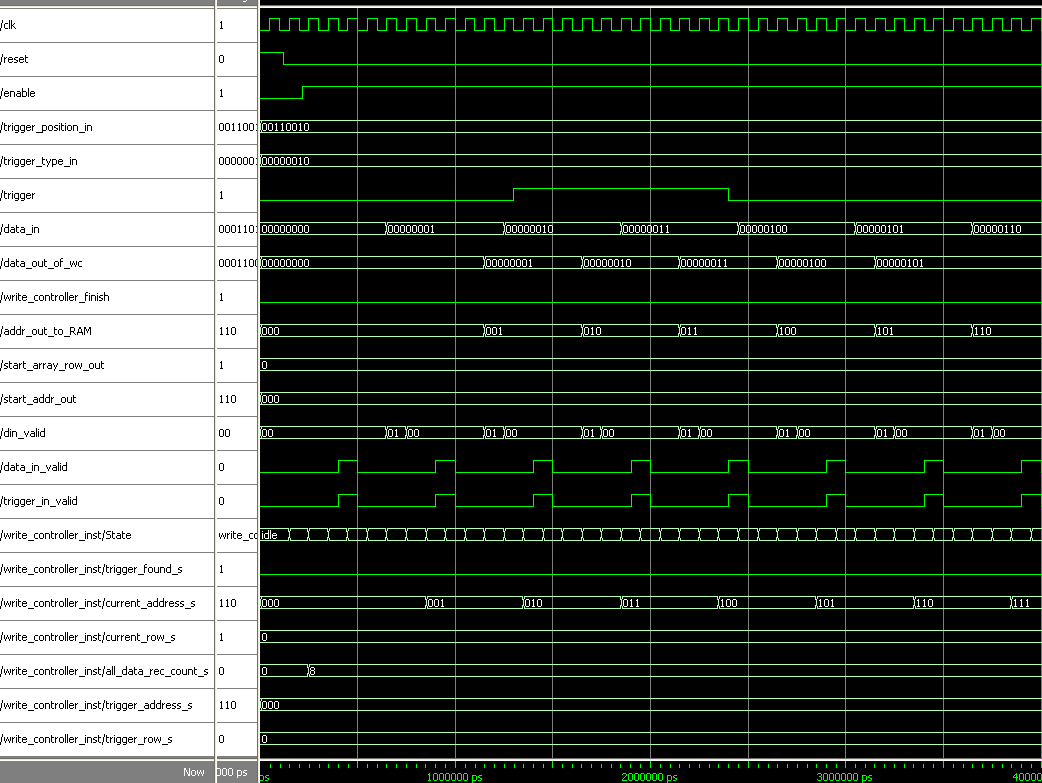
-width of a single RAM-8

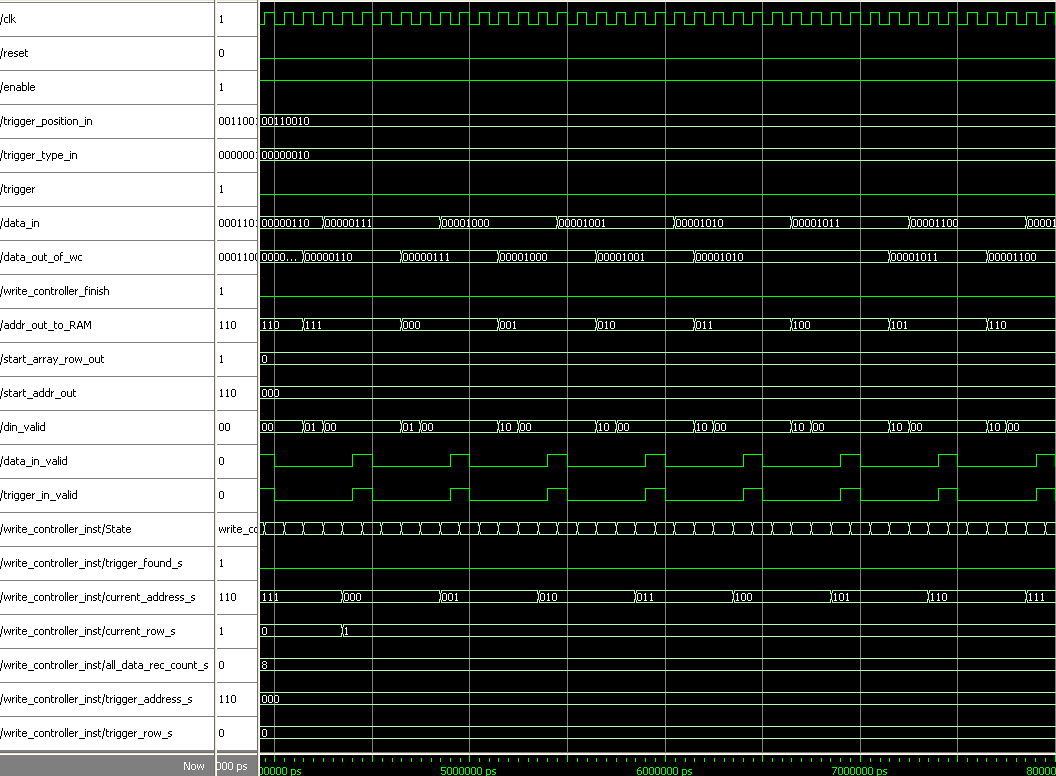
-numbers of signals for recording-8

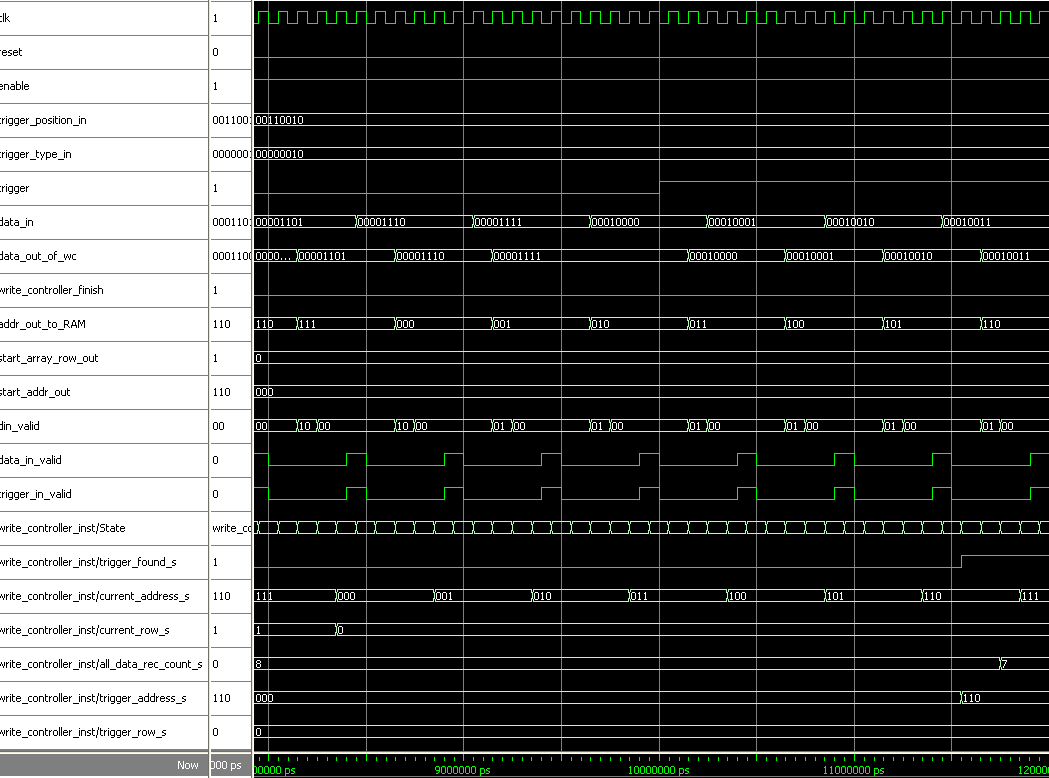
It takes two RAMs to record the entire information.

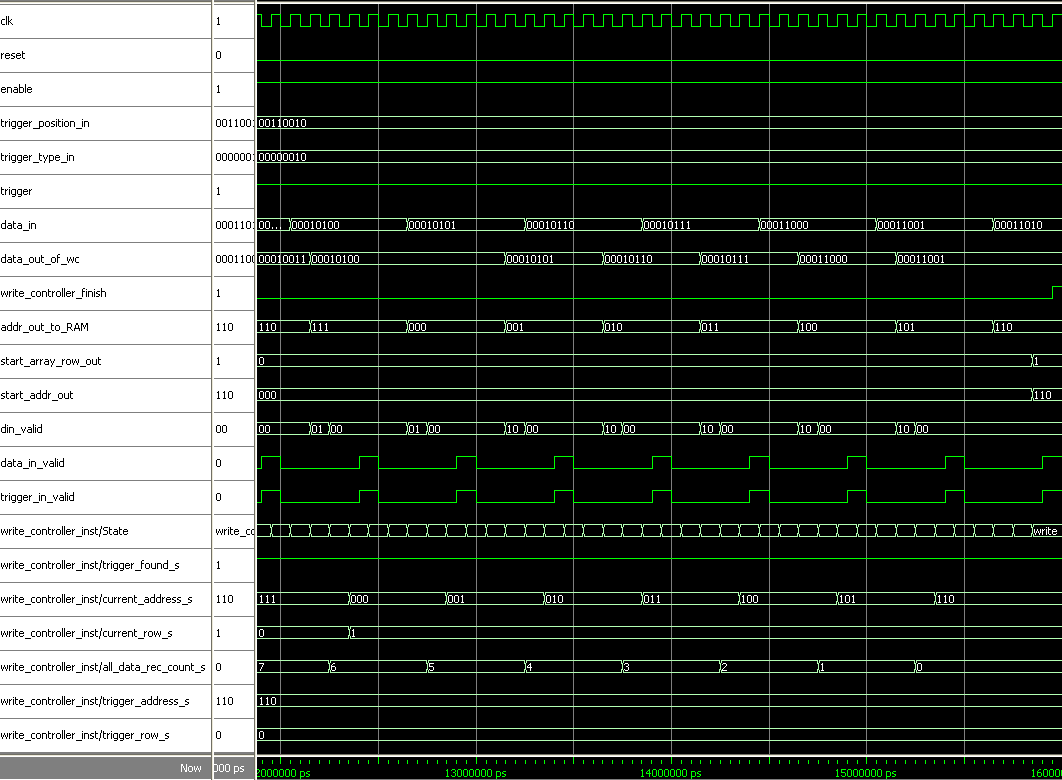
When we enable the first RAM, din\_valid=01, when we enable the second RAM, din\_valid=10. They both rise for one clock cycle in each recording cycle, the rest of the time it will be 00.

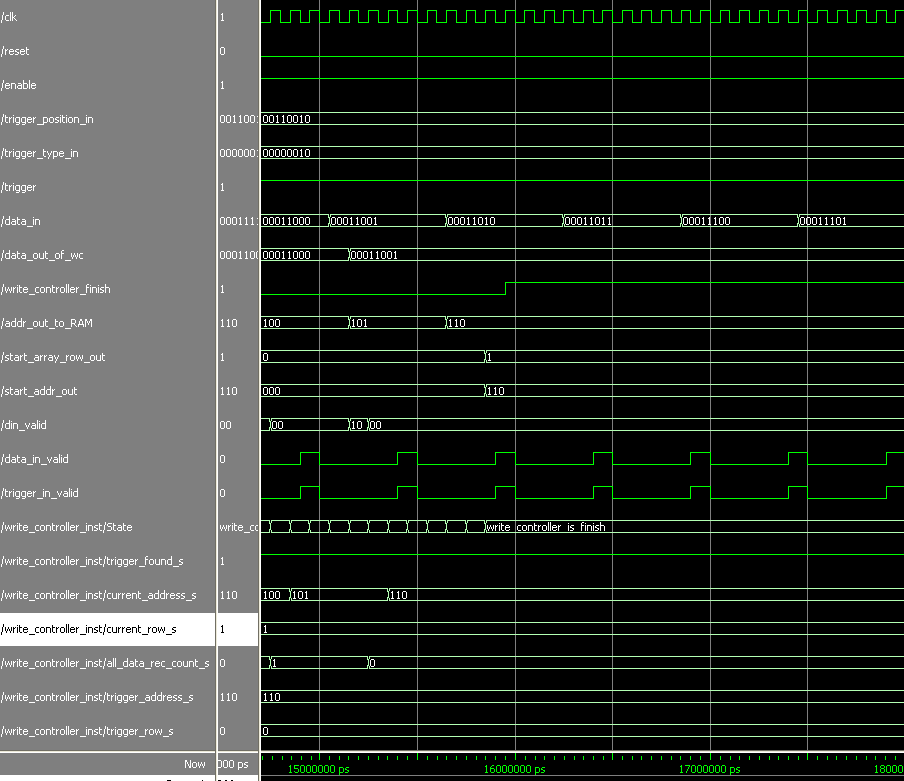
Simulation:











Analysis :

First we can see that trigger is found at address 110 in row 0, because of 50% trigger position we expect that the start address will be also 110 but in the other row (row 1) and that is exactly the outcome. We also see that trigger is rise just after we detect three continuous trigger at high mode and even that after that the trigger is still high, meaning that we found another trigger rise, the system doesn’t refer that and stay with the initial address.

TEST NUMBER 3

Generics values:

|  |  |  |
| --- | --- | --- |
| Comments | Value | Name |
|  | 1 | reset\_polarity\_g |
|  | 1 | enable\_polarity\_g |
| Each the number og addresses is RAM in | 3 | signal\_ram\_depth\_g |
| "word" width – line in the RAM | 8 | signal\_ram\_width\_g |
| The number of recorded signals is | 4 | record\_depth\_g |
| BUS width of the information entering the component | 8 | data\_width\_g |
| Word width in WB protocol | 8 | Add\_width\_g |
| Number of signals we record in each iteration | 8 | num\_of\_signals\_g |

Variables values:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Comments | Value | | | Name |
| Inputs | | | | |
|  | 50 duty cycle | | | clk |
|  | 120-20000 | | 0-120 | Reset |
| 0 | | 1 |
|  | 220-20000 | | 0-220 | Enable |
| 1 | | 0 |
| 25 % | 00011001 | | | Trigger position in |
| rise | 00000000 | | | Trigger type in |
| Counter- 500 time period | 0-39 | | | data\_in |
|  | 10000-20000 | | 0-10000 | trigger |
| 1 | | 0 |
| Come from WB. repeater | 400-500 | | 0-400 | data\_in\_valid |
| 1 | | 0 |
| Come from WB. repeater | 400-500 | | 0-400 | trigger\_in\_valid |
| 1 | | 0 |
| Outputs | | | | |
| When data\_in\_valid and trigger\_in\_valid signals rise at stste send\_out\_data\_and\_addr, data out is been update | Update every 500 ns  (5 clk cycles) | | | Data out of wc |
| When data\_in\_valid and trigger\_in\_valid signals rise at stste send\_out\_data\_and\_addr, addr out is been update | Update every 500 ns  (5 clk cycles) | | | addr\_out\_to\_RAM |
| Rise when we recorded all the data. 4 record cycles after trigger rise | 17000-20000 | 0-17000 | | write\_controller\_finish |
| 1 | 0 | |
| When trigger is found and all data is recorded, we send out the address of the relevant data in the RAM. This time, 000 is the correct address | 16850-20000 | 0-16850 | | start\_addr\_out |
| 000 | 0 | |
| When trigger is found and all data is recorded, we send out the array row of the relevant data in the RAM | 16850-20000 | 0-16850 | | start\_array\_row\_out |
| 1 | 0 | |
| Length is number of RAMs, to enable the N RAM we put 1 in the N place and all the other is 0 | Enable the correct RAM when we send the data and address out | | | din\_valid |

Explanation:

The trigger type is set to 'rise'. The information will be recorded after trigger rise, meaning from the moment the trigger rises we'll wait 4 recording cycles (each cycle is 5 clk cycles), then we'll extract the start address to the next component.

Recording cycle:

1. The information is being sampled.
2. Check whether there was a trigger rise.
3. Sending relevant information and address to the RAM.
4. Check whether the information was recorded entirely.
5. In case there is missing information- calculate the next address.
6. In case the information has been recorded properly- calculate the start address of the relevant information.

Description of the RAM composition:

-information depth of single RAM- 8

-information depth needed for recordind-16

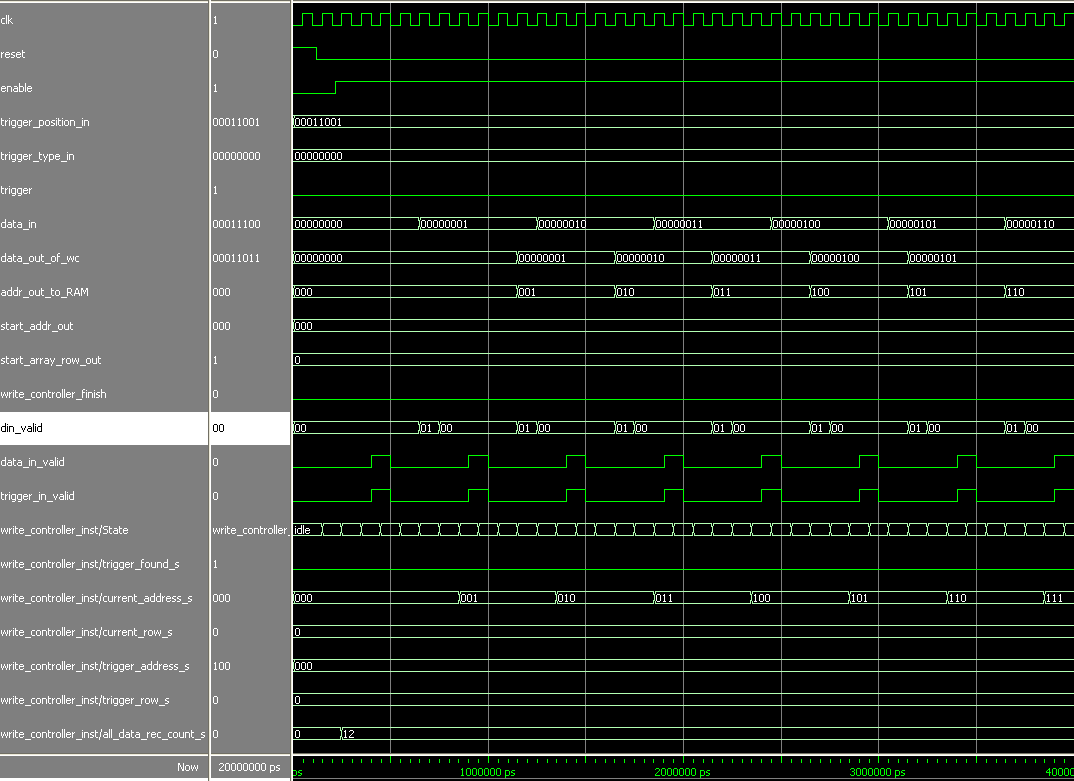
-width of a single RAM-8

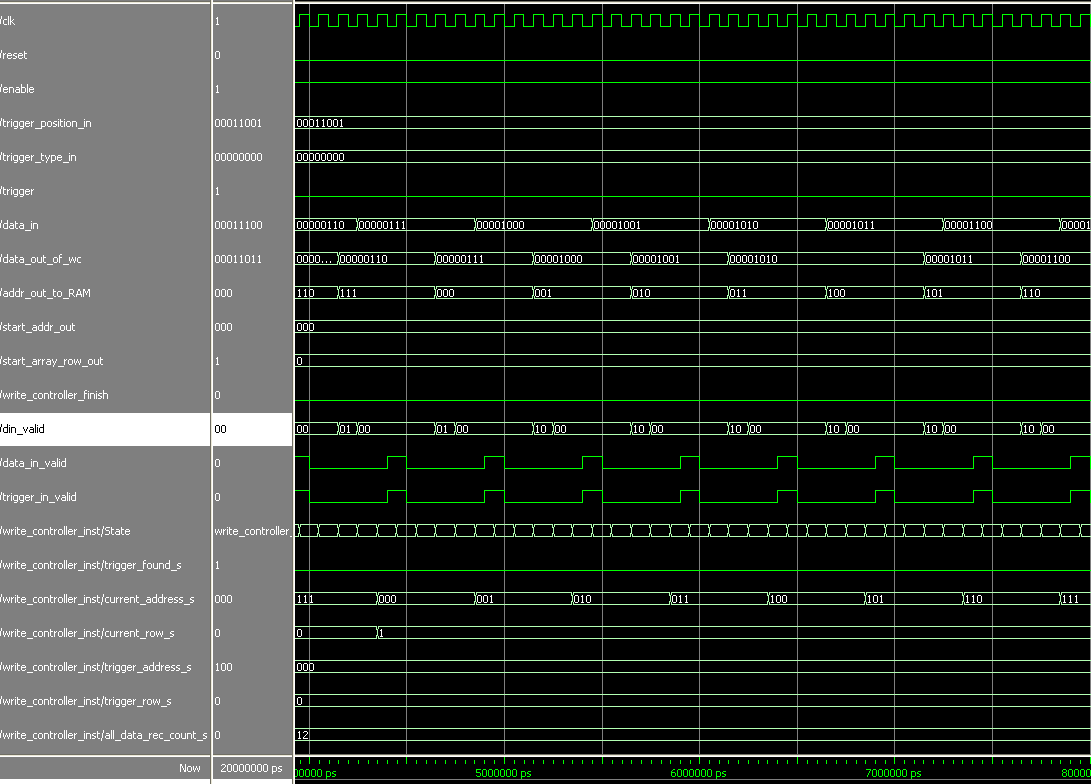
-numbers of signals for recording-8

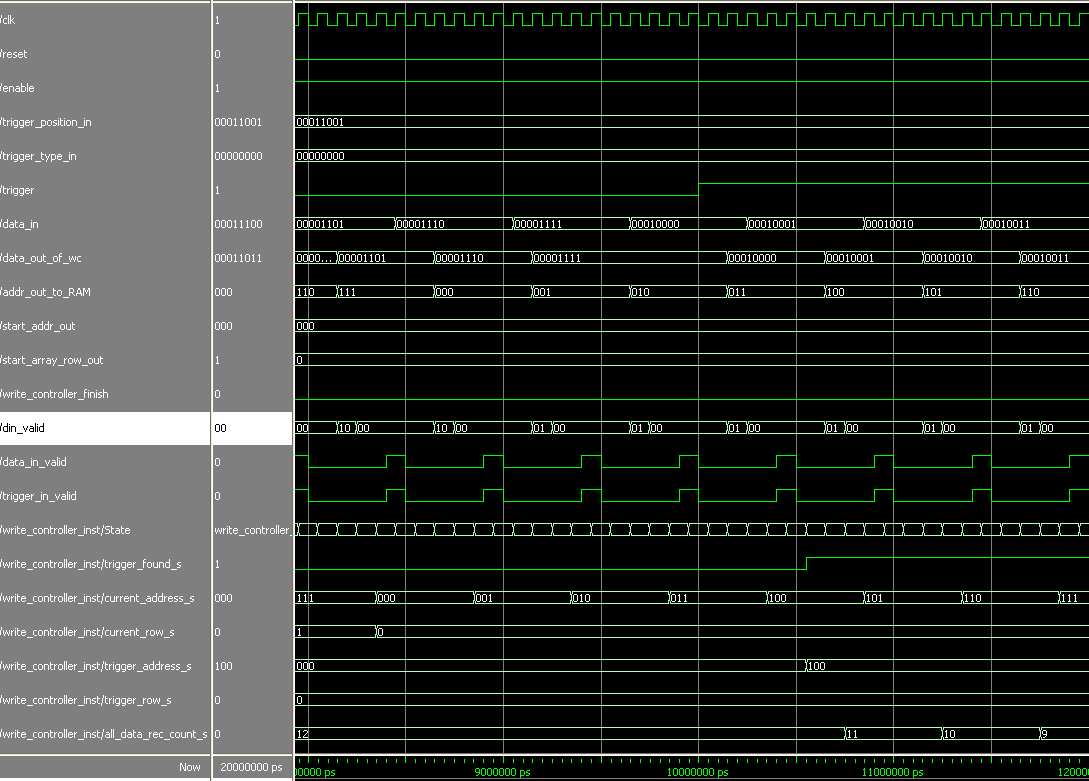
It takes two RAMs to record the entire information.

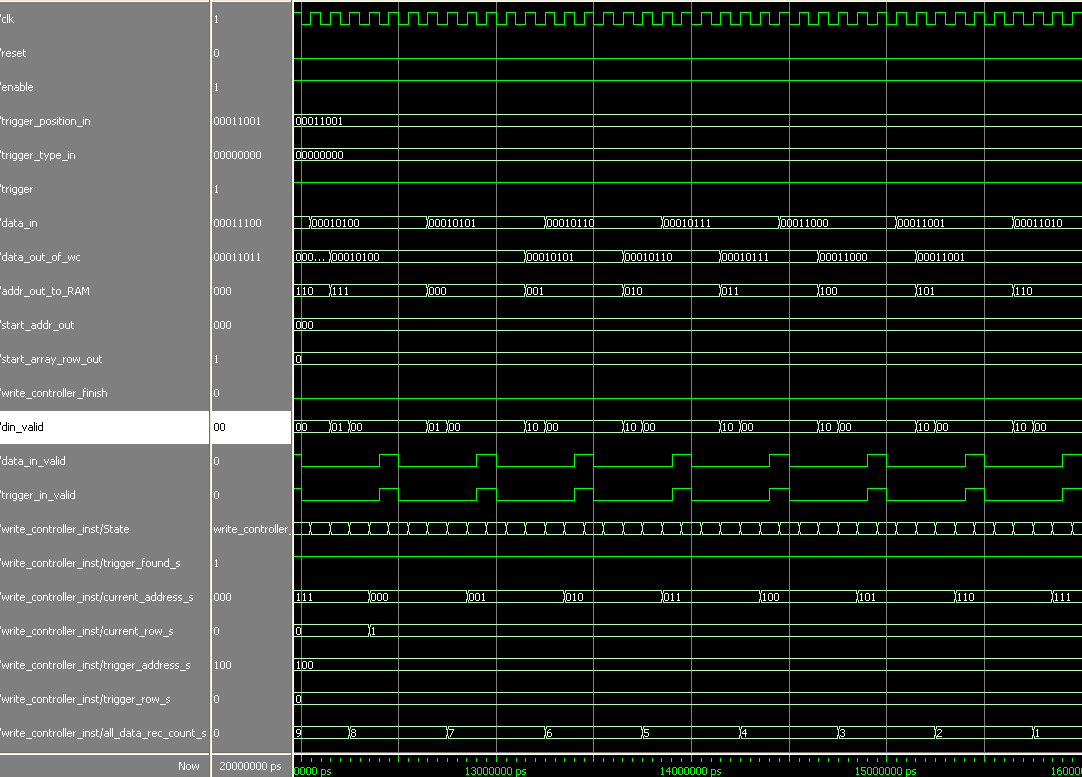
When we enable the first RAM, din\_valid=01, when we enable the second RAM, din\_valid=10. They both rise for one clock cycle in each recording cycle, the rest of the time it will be 00.

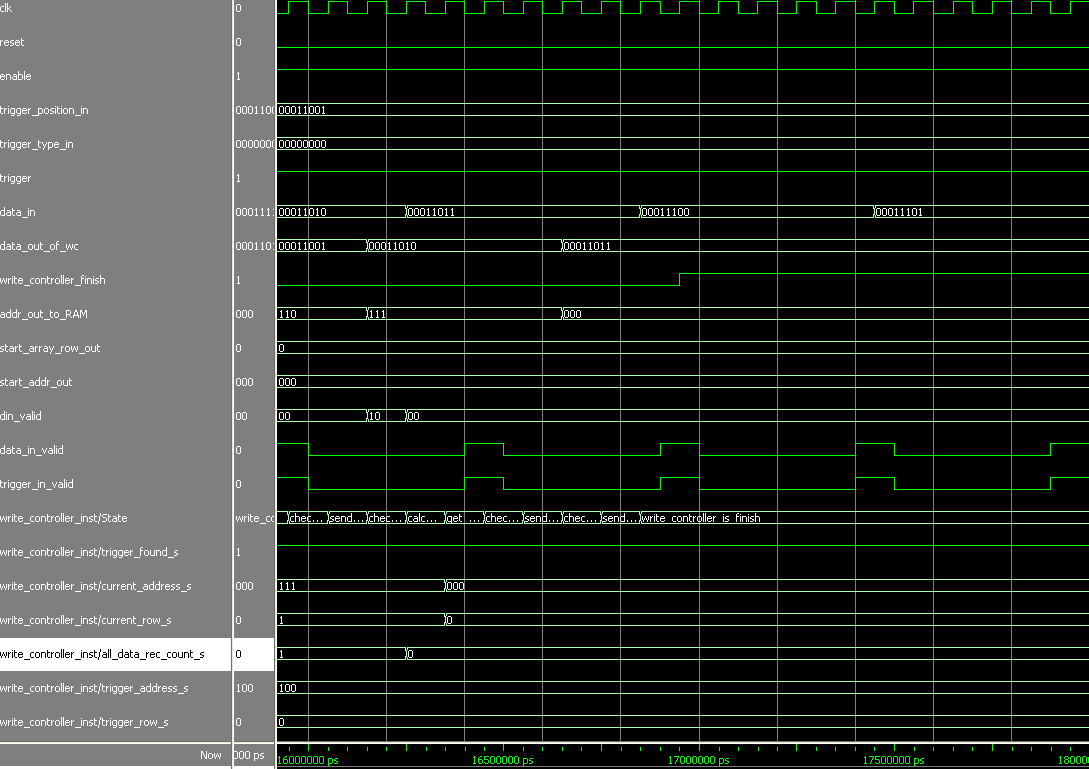
Simulation:











Analysis :

After trigger rise (10000 ns), the system identify that and rise trigger\_foud\_s. since that, we count 12 record cycles (trigger\_position is 25, so 75 % of recorded data will be after trigger rise) until the system finish recording the hole data. Trigger address is 100 (4) in first RAM (row 0) and therefore the start address will be 12+4 = 16 -> 000 in the first RAM.

TEST NUMBER 4

Generics values:

|  |  |  |
| --- | --- | --- |
| Comments | Value | Name |
|  | 1 | reset\_polarity\_g |
|  | 1 | enable\_polarity\_g |
| Each the number og addresses is RAM in | 3 | signal\_ram\_depth\_g |
| "word" width – line in the RAM | 8 | signal\_ram\_width\_g |
| The number of recorded signals is | 4 | record\_depth\_g |
| BUS width of the information entering the component | 8 | data\_width\_g |
| Word width in WB protocol | 8 | Add\_width\_g |
| Number of signals we record in each iteration | 8 | num\_of\_signals\_g |

Variables values:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Comments | Value | | | Name |
| Inputs | | | | |
|  | 50 duty cycle | | | clk |
|  | 120-20000 | | 0-120 | Reset |
| 0 | | 1 |
|  | 220-20000 | | 0-220 | Enable |
| 1 | | 0 |
| 50% | 00110010 | | | Trigger position in |
| One (3 high) | 00000010 | | | Trigger type in |
| Counter- 500 time period | 0-39 | | | data\_in |
|  | 10000-20000 | | 0-10000 | trigger |
| 1 | | 0 |
| Come from WB. repeater | 400-500 | | 0-400 | data\_in\_valid |
| 1 | | 0 |
| Come from WB. repeater | 400-500 | | 0-400 | trigger\_in\_valid |
| 1 | | 0 |
| Outputs | | | | |
| When data\_in\_valid and trigger\_in\_valid signals rise at stste send\_out\_data\_and\_addr, data out is been update | Update every 500 ns  (5 clk cycles) | | | Data out of wc |
| When data\_in\_valid and trigger\_in\_valid signals rise at stste send\_out\_data\_and\_addr, addr out is been update | Update every 500 ns  (5 clk cycles) | | | addr\_out\_to\_RAM |
| Rise when we recorded all the data | 11500-20000 | 0-11500 | | write\_controller\_finish |
| 1 | 0 | |
| When trigger is found and all data is recorded, we send out the address of the relevant data in the RAM | 11400-20000 | 0-11400 | | start\_addr\_out |
| 101 | 0 | |
| When trigger is found and all data is recorded, we send out the array row of the relevant data in the RAM | 11400-20000 | 0-11400 | | start\_array\_row\_out |
| 0 | 0 | |
| Length is number of RAMs, to enable the N RAM we put 1 in the N place and all the other is 0 | Enable the correct RAM when we send the data and address out | | | din\_valid |

Explanation:

The trigger type is set to 'one'. The information will be recorded after trigger will be in high mode for 3 cycles. From the moment that we will find trigger rise we'll wait 8 recording cycles (each cycle is 5 clk cycles), then we'll extract a start address to the next component.

Recording cycle:

1. The information is being sampled.
2. Check whether there was a trigger rise.
3. Sending relevant information and address to the RAM.
4. Check whether the information was recorded entirely.
5. In case there is missing information- calculate the next address.
6. In case the information has been recorded properly- calculate the start address of the relevant information.

Description of the RAM composition:

-information depth of single RAM- 8

-information depth needed for recordind-16

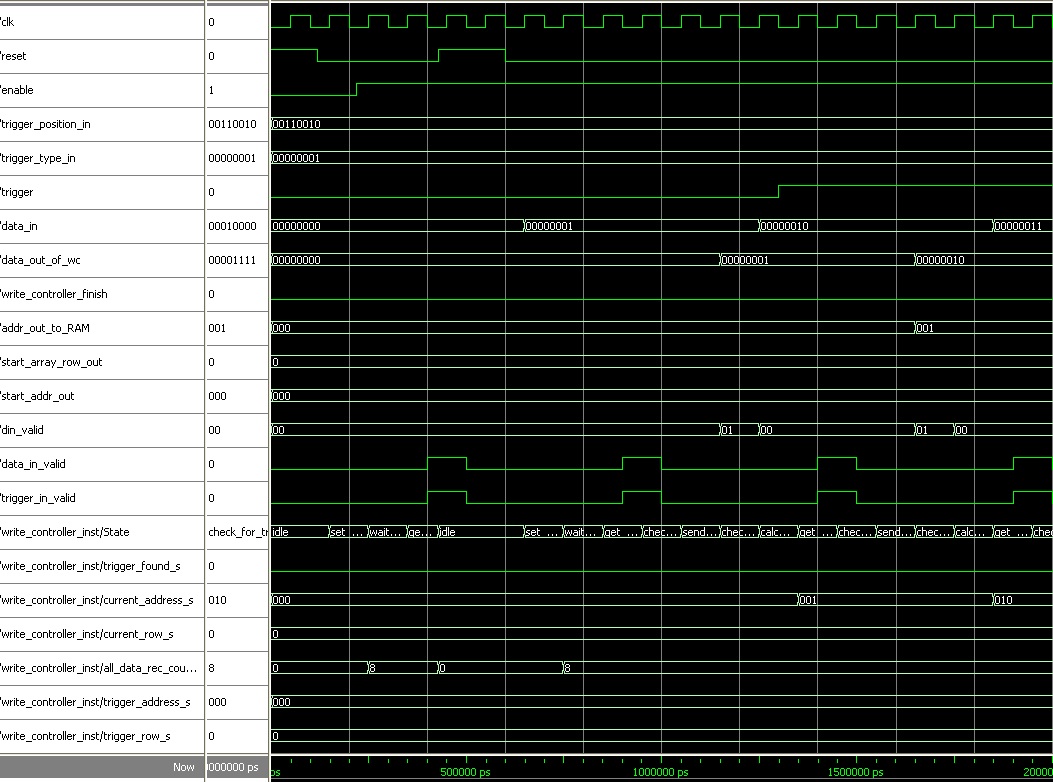
-width of a single RAM-8

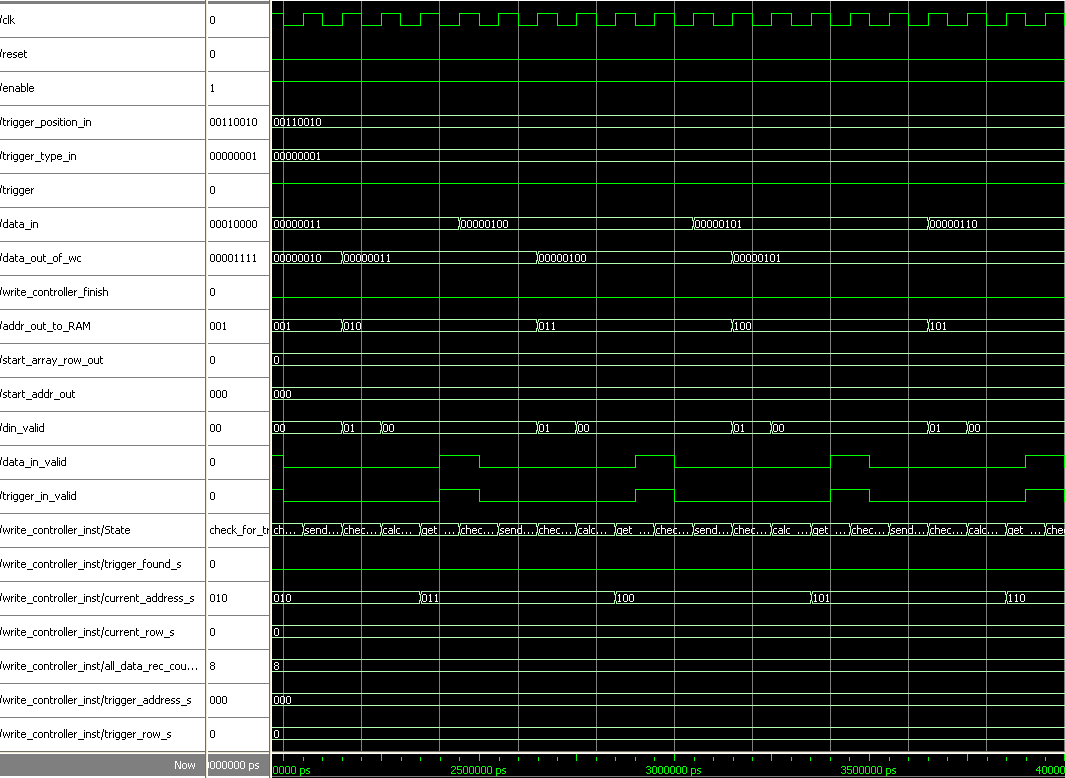
-numbers of signals for recording-8

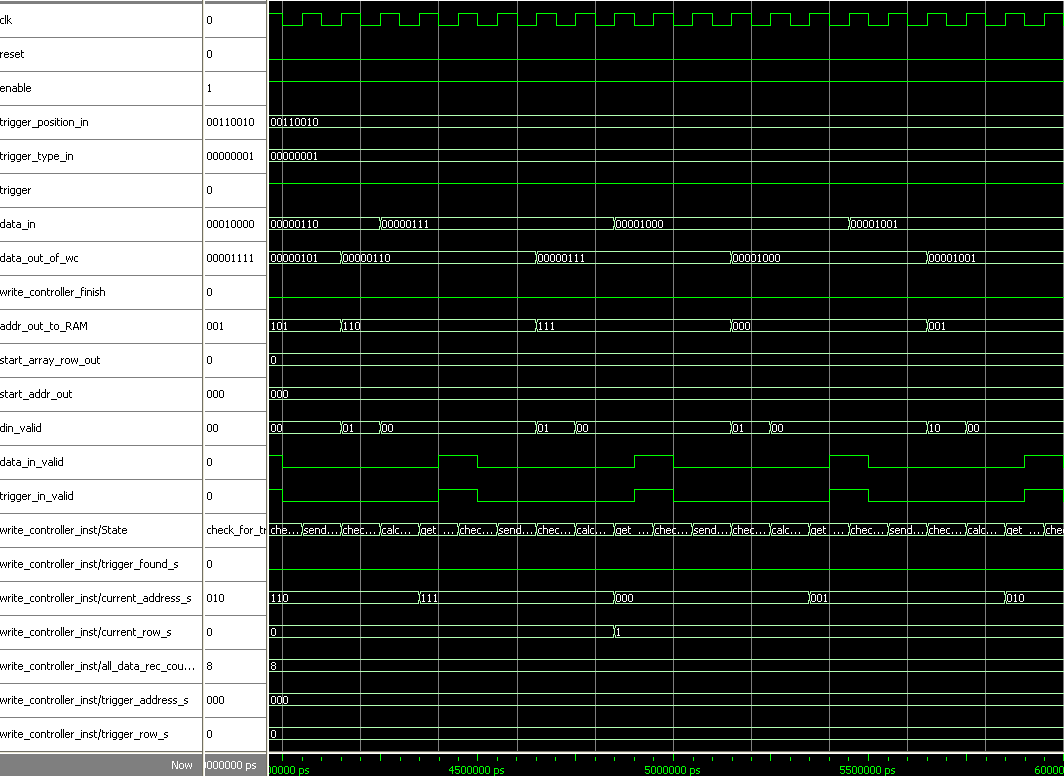
It takes two RAMs to record the entire information.

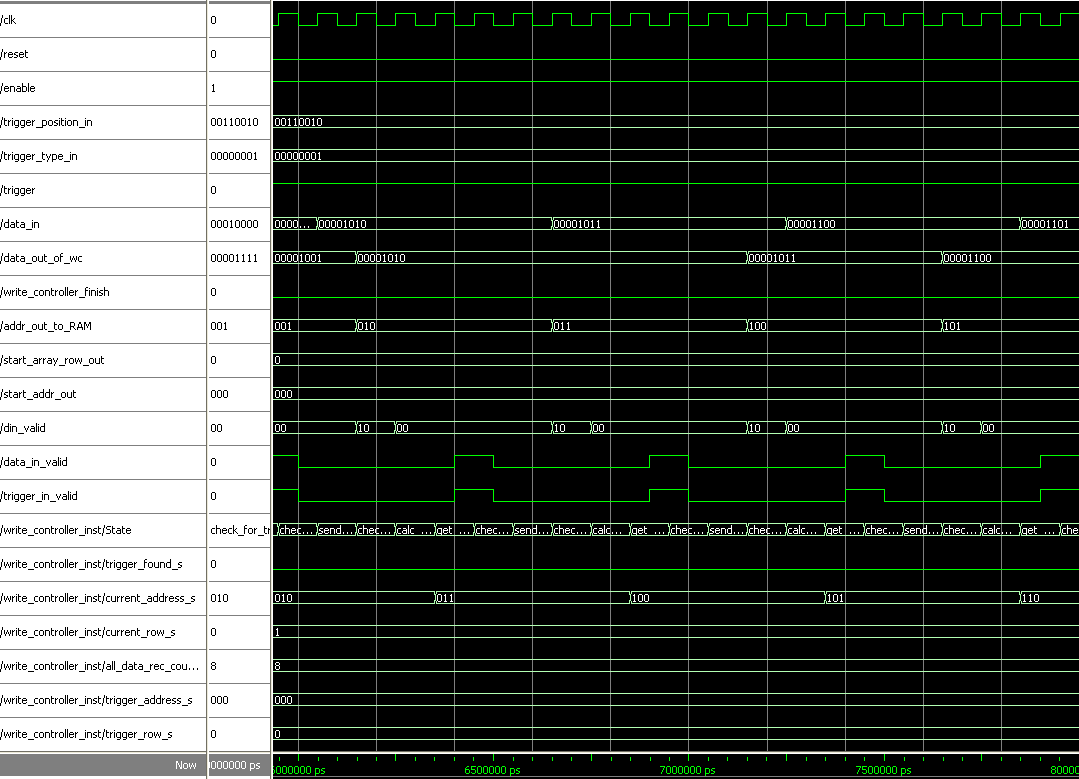
When we enable the first RAM, din\_valid=01, when we enable the second RAM, din\_valid=10. They both rise for one clock cycle in each recording cycle, the rest of the time it will be 00.

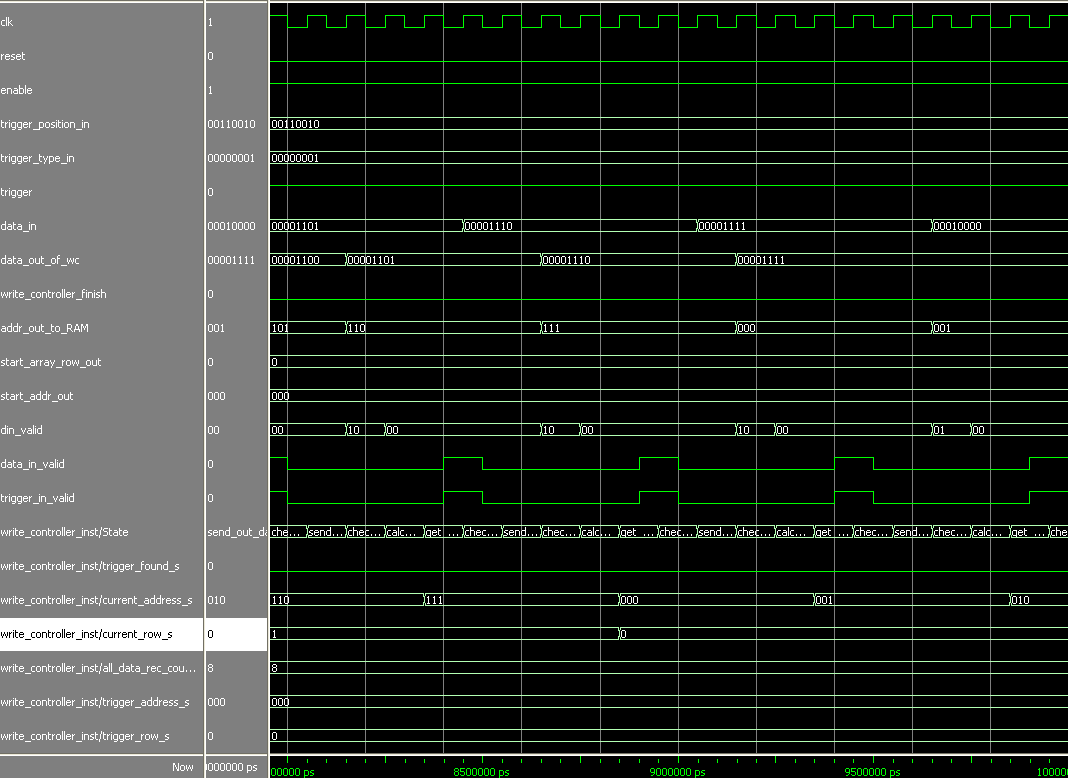
Simulation:

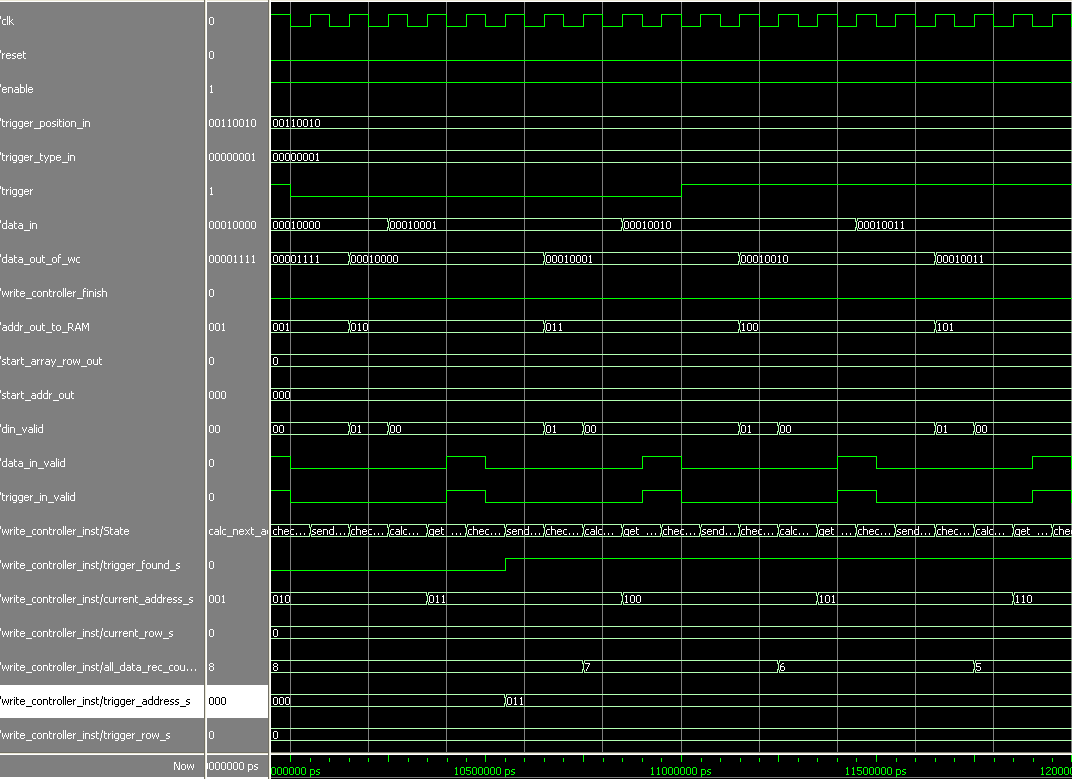


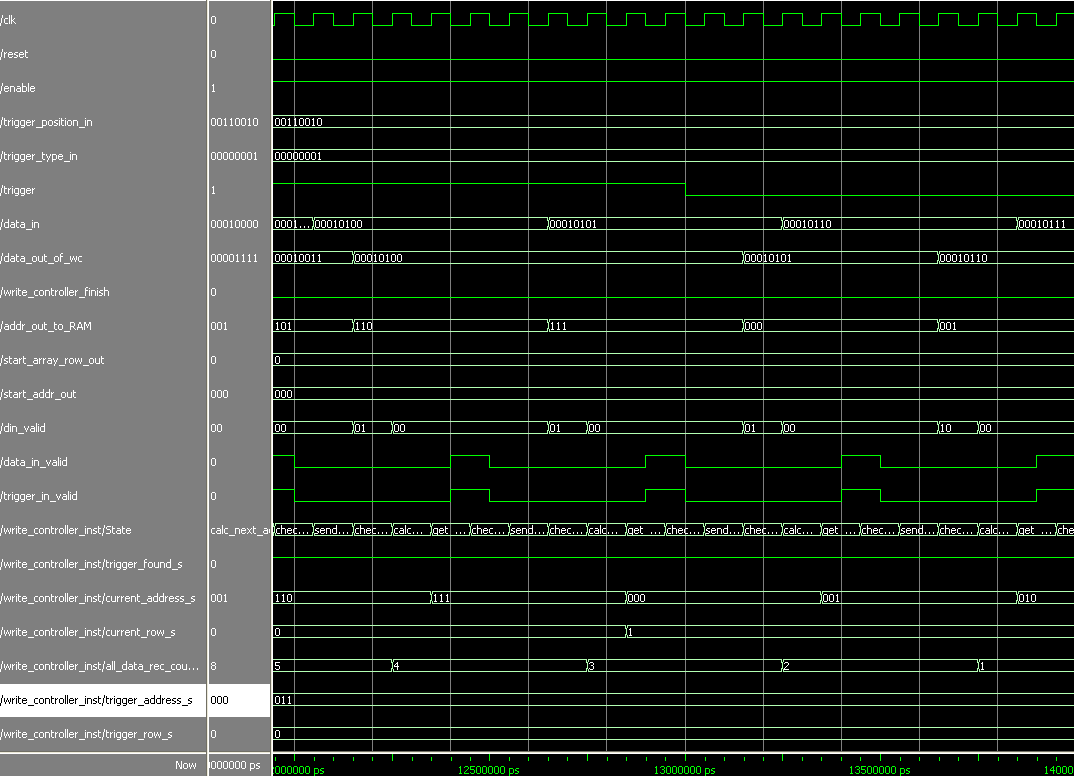


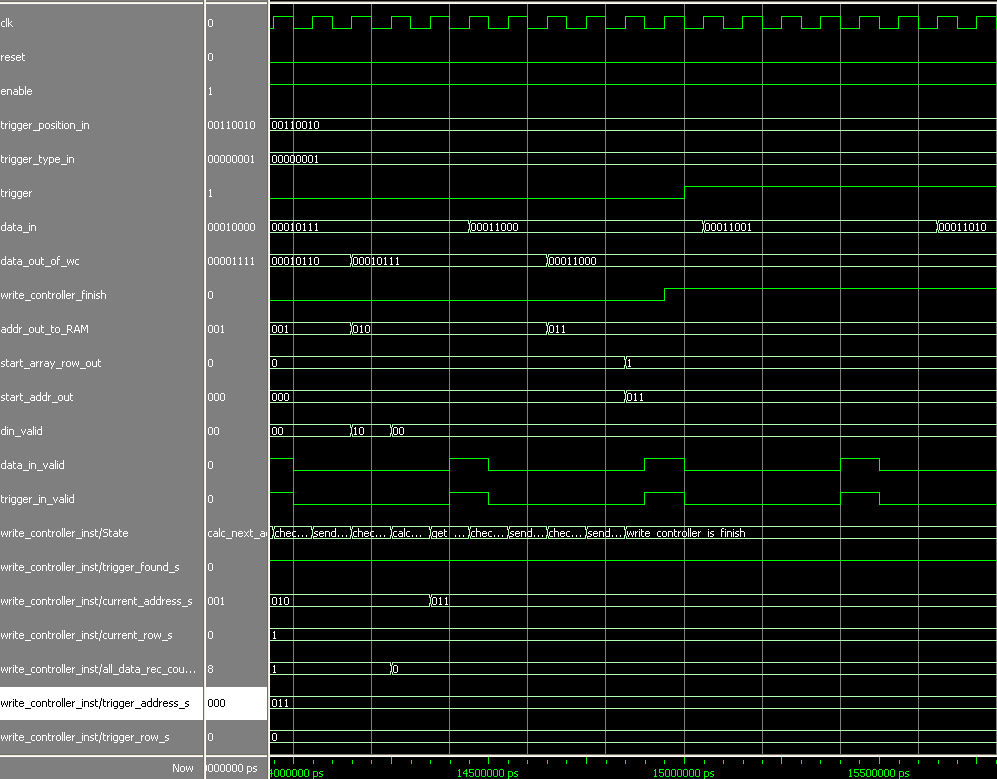












Analysis :

We see that trigger low at first, but trigger\_found is not rise. Just after trigger is fall (change from high to low, at 10000 ns) trigger\_found rise. Trigger address is at 011 in row 0, because of 50% trigger position we expect that the start address will be also 011 but in the other row (row 1) and that is exactly the outcome. We rise reset signal after 500 ns and the system returns to idle state. Trigger is fall again at 13000 ns, but since trigger was already found, we ignore that.