TEST NUMBER 1

Generics values:

|  |  |  |
| --- | --- | --- |
| Comments | Value | Name |
|  | 1 | reset\_polarity\_g |
|  | 1 | enable\_polarity\_g |
| Each the number og addresses is RAM in | 3 | signal\_ram\_depth\_g |
| "word" width – line in the RAM | 8 | signal\_ram\_width\_g |
| The number of recorded signals is | 4 | record\_depth\_g |
| BUS width of the information entering the component | 8 | data\_width\_g |
| Word width in WB protocol | 8 | Add\_width\_g |
| Number of signals we record in each iteration | 8 | num\_of\_signals\_g |

Variables values:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Comments | Value | | | | | | | Name |
| Inputs | | | | | | | | |
|  | 50 duty cycle | | | | | | | clk |
|  | 6000-20000 | 5500-6000 | | 120-5500 | | | 0-120 | Reset |
| 0 | 1 | | 0 | | | 1 |
|  | 18000-20000 | 15000-18000 | | 220-15000 | | | 0-220 | Enable |
| 1 | 0 | | 1 | | | 0 |
| Precentage of data recorded after trigger rise | 00000000 | | | | | | | Trigger position in |
| rise | 00000000 | | | | | | | Trigger type in |
| Counter | 0-150 | | | | | | | data\_in |
|  | 10000-20000 | | | | 0-10000 | | | trigger |
| 1 | | | | 0 | | |
| Outputs | | | | | | | | |
|  | Update every clk cycle | | | | | | | Data out of wc |
|  | Update every clk cycle | | | | | | | addr\_out\_to\_RAM |
| Rise when we recorded all the data, fall after we start a new recording cycle | 15150-20000 | | 12050-15150 | | | 0-12050 | | write\_controller\_finish |
| 0 | | 1 | | | 0 | |
| When trigger is found and all data is recorded, we send out the address of the relevant data in the RAM | 15150-20000 | | 11950-15150 | | | 0-11950 | | start\_addr\_out |
| 000 | | 110 | | | 000 | |
| When trigger is found and all data is recorded, we send out the array row of the relevant data in the RAM | 15150-20000 | | 11950-15150 | | | 0-11950 | | start\_array\_row\_out |
| 0 | | 0 | | | 0 | |
| Length is number of RAMs, to enable the N RAM we put 1 in the N place and all the other is 0 | Enable the correct RAM when we send the data and address out | | | | | | | din\_valid |

Explanation:

The trigger type is set to 'rise'. The information will be recorded entirely after trigger rise,meaning from the moment the trigger rises we'll wait 16 clock cycles, then we'll extract an address to the next component. We can also see that as soon as the recording has finished and enable was set to '0', the system returns to 'idle' mode and a new recording cycle is starting.

Description of the RAM composition:

-information depth of single RAM- 8

-information depth needed for recordind-16

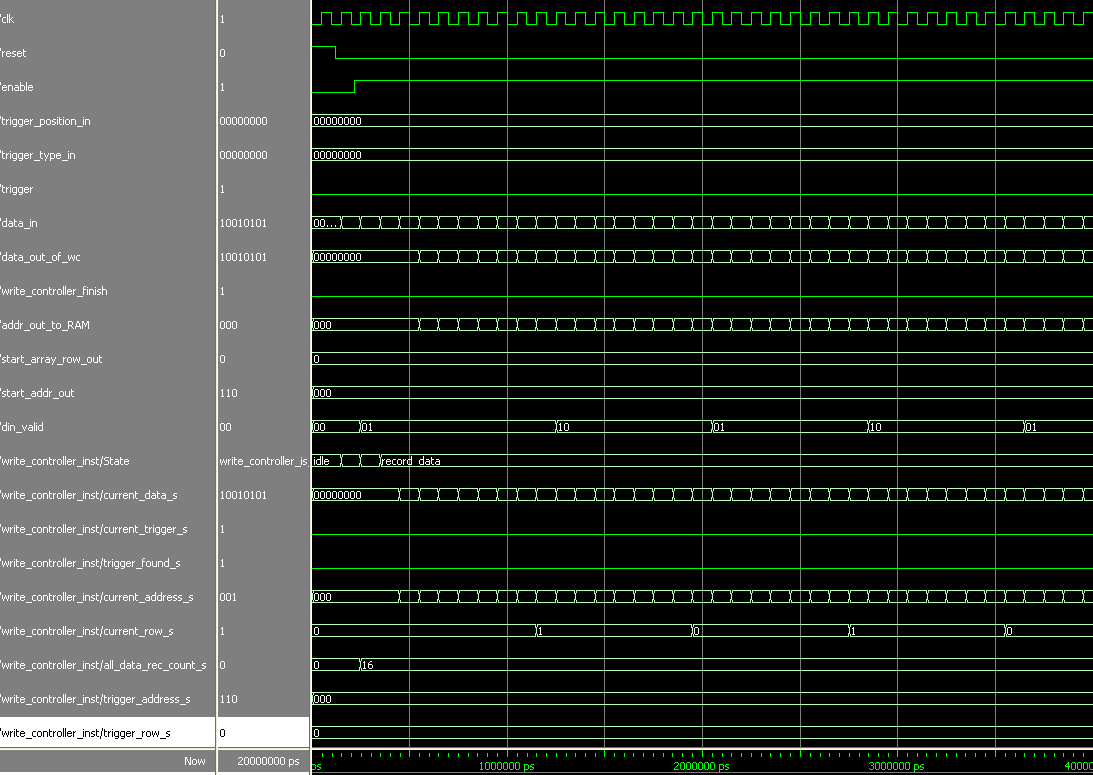
-width of a single RAM-8

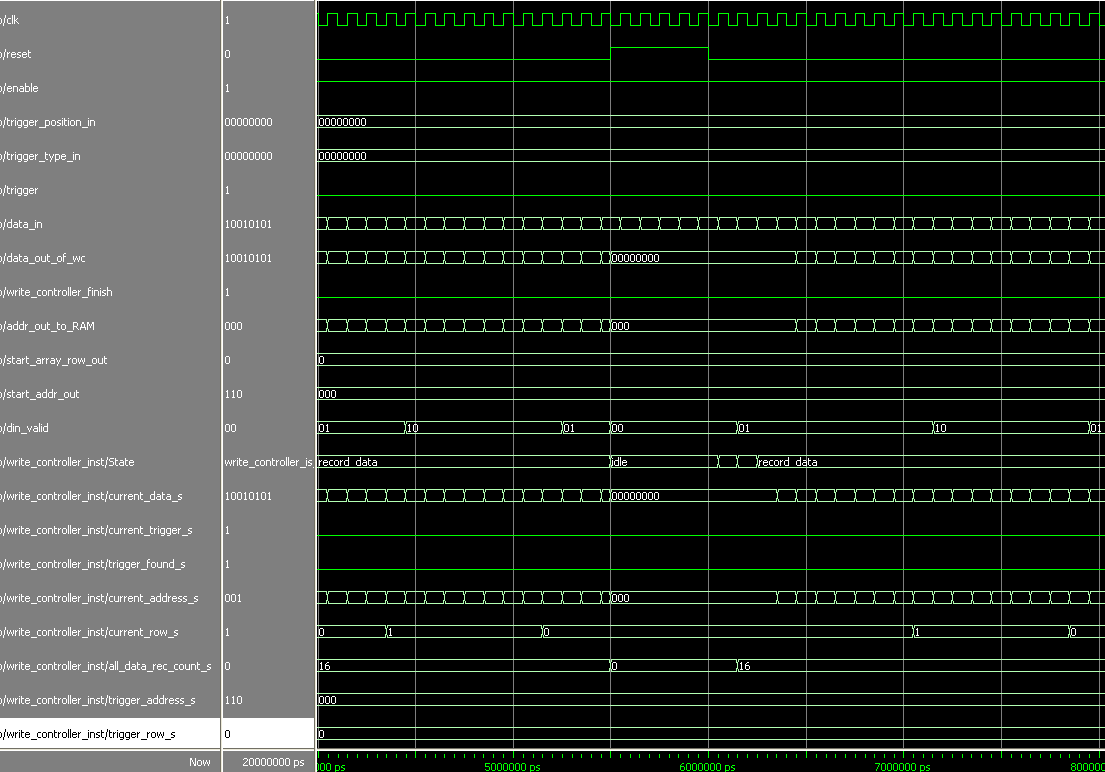
-numbers of signals for recording-8

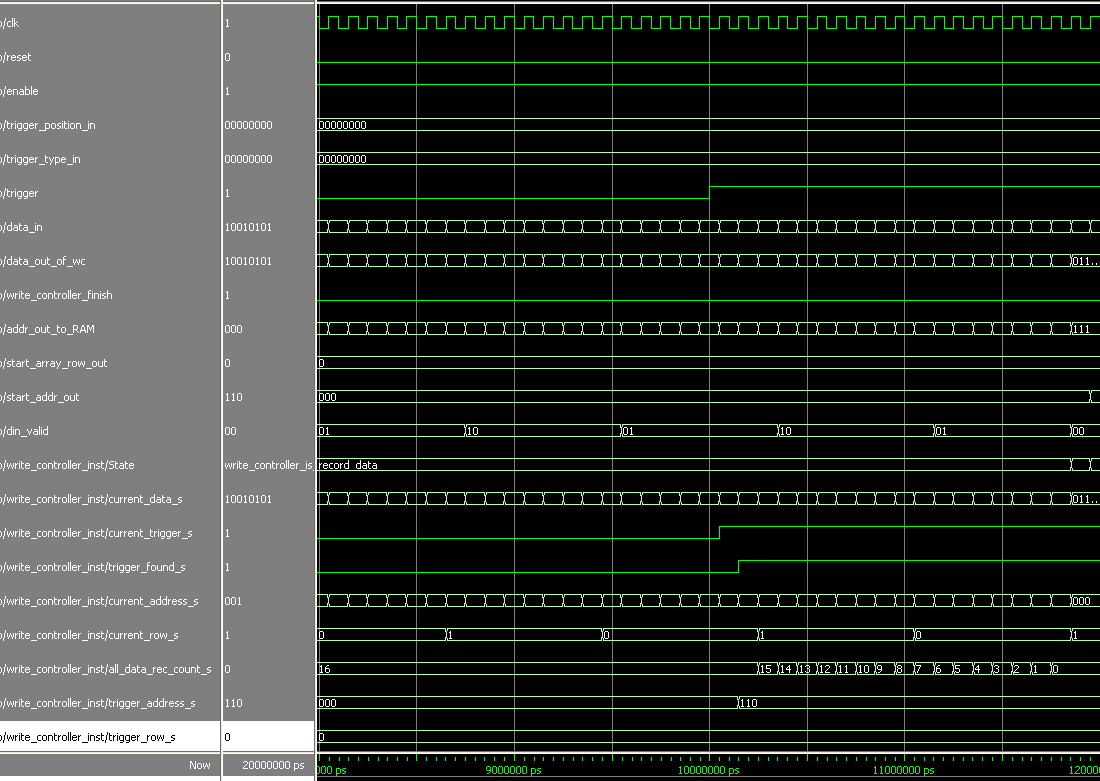
It takes two RAMs to record the entire information.

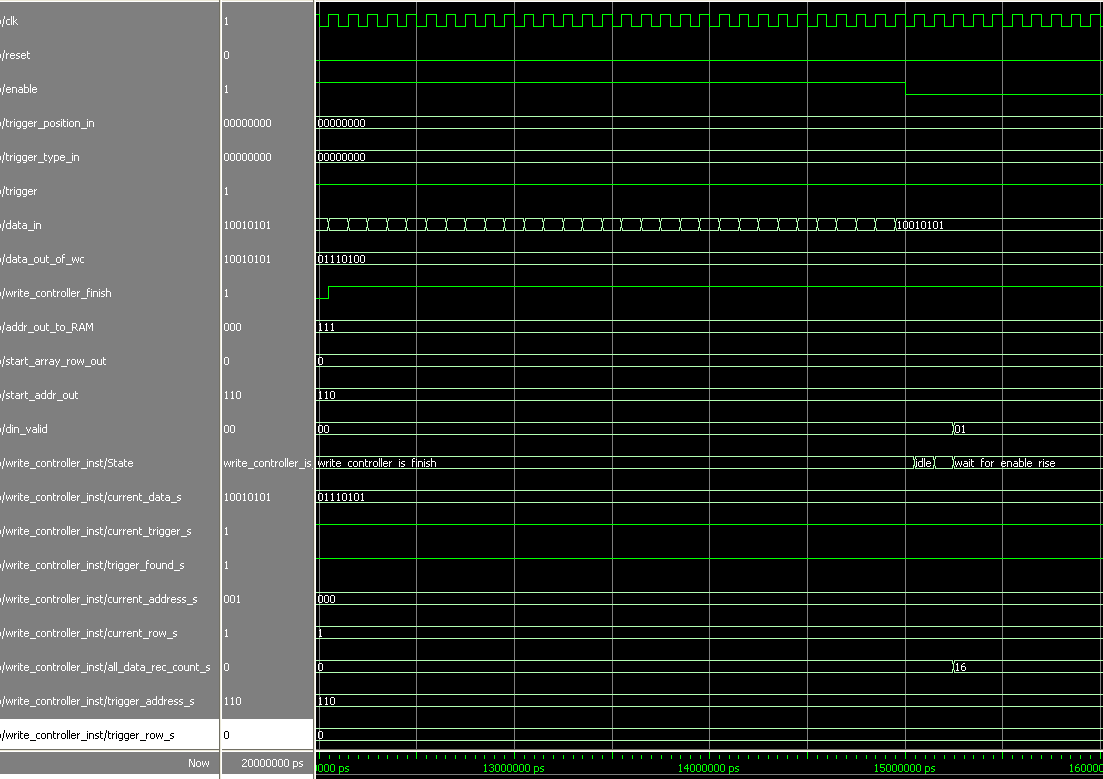
When we enable the first RAM, din\_valid=01, when we enable the second RAM, din\_valid=10. They both rise for one clock cycle in each recording cycle, the rest of the time it will be 00.

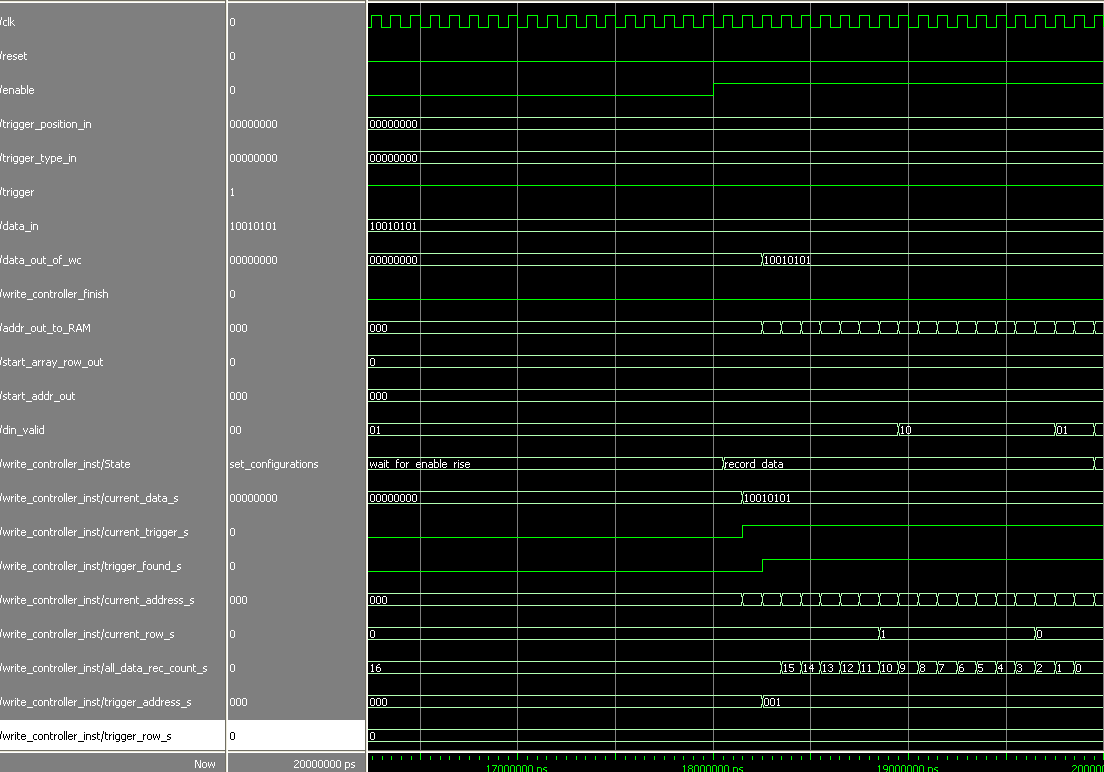
Simulation:











Analysis:

the trigger type is rise. Trigger position is 0. Once trigger rises, we wait 16 cycles to record. The rising address is being sampled and a start address for the next component is being calculated. As soon as the recording is finished we'll wait for enable fall. Then the system start all over again as we can see.

TEST NUMBER 2

Generics values:

|  |  |  |
| --- | --- | --- |
| Comments | Value | Name |
|  | 1 | reset\_polarity\_g |
|  | 1 | enable\_polarity\_g |
| Each the number og addresses is RAM in | 3 | signal\_ram\_depth\_g |
| "word" width – line in the RAM | 8 | signal\_ram\_width\_g |
| The number of recorded signals is | 4 | record\_depth\_g |
| BUS width of the information entering the component | 8 | data\_width\_g |
| Word width in WB protocol | 8 | Add\_width\_g |
| Number of signals we record in each iteration | 8 | num\_of\_signals\_g |

Variables values:

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Comments | Value | | | | | | | | | | | Name |
| Inputs | | | | | | | | | | | | |
|  | 50 duty cycle | | | | | | | | | | | clk |
|  | 120-20000 | | | | | 0-120 | | | | | | Reset |
| 0 | | | | | 1 | | | | | |
| Second time that enable is low, the system starting a new recording cycle | 18000-20000 | | 15000-18000 | | | 220-15000 | | | 0-220 | | | Enable |
| 1 | | 0 | | | 1 | | | 0 | | |
| 50% | 00110010 | | | | | | | | | | | Trigger position in |
| One (3 high) | 00000010 | | | | | | | | | | | Trigger type in |
| Counter | 0-150 | | | | | | | | | | | data\_in |
| Trigger is defined as 3 high | 15000-20000 | 13000-15000 | | | 11000-13000 | 10000-11000 | | 9800-10000 | | | 0-9800 | trigger |
| 1 | 0 | | | 1 | 0 | | 1 | | | 0 |
| Outputs | | | | | | | | | | | | |
|  | Update every clock cycle | | | | | | | | | | | Data out of wc |
|  | Update every clock cycle | | | | | | | | | | | addr\_out\_to\_RAM |
| Rise when we recorded all the data | 19500-20000 | | | 15100-19500 | | | 12500-15100 | | | 0-12500 | | write\_controller\_finish |
| 1 | | | 0 | | | 1 | | | 0 | |
| When trigger is found and all data is recorded, we send out the address of the relevant data in the RAM | 19500-20000 | | | 15100-19500 | | | 12300-15100 | | | 0-12300 | | start\_addr\_out |
| 011 | | | 000 | | | 101 | | | 000 | |
| When trigger is found and all data is recorded, we send out the array row of the relevant data in the RAM | 19500-20000 | | | 15100-19500 | | | 12300-15100 | | | 0-12300 | | start\_array\_row\_out |
| 1 | | | 0 | | | 0 | | | 0 | |
| Length is number of RAMs, to enable the N RAM we put 1 in the N place and all the other is 0 | Enable the correct RAM when we send the data and address out | | | | | | | | | | | din\_valid |

Explanation:

The trigger type is set to 'one'. The information will be recorded after trigger will be in high mode for 3 cycles. From the moment that we will find trigger rise we'll wait 8 clock cycles (50% of total 16 units), then we'll extract a start address to the next component. Because trigger position is 50, the start address will be exactly like the trigger address, but the trigger row out will be the opposite one.

Description of the RAM composition:

-information depth of single RAM- 8

-information depth needed for recordind-16

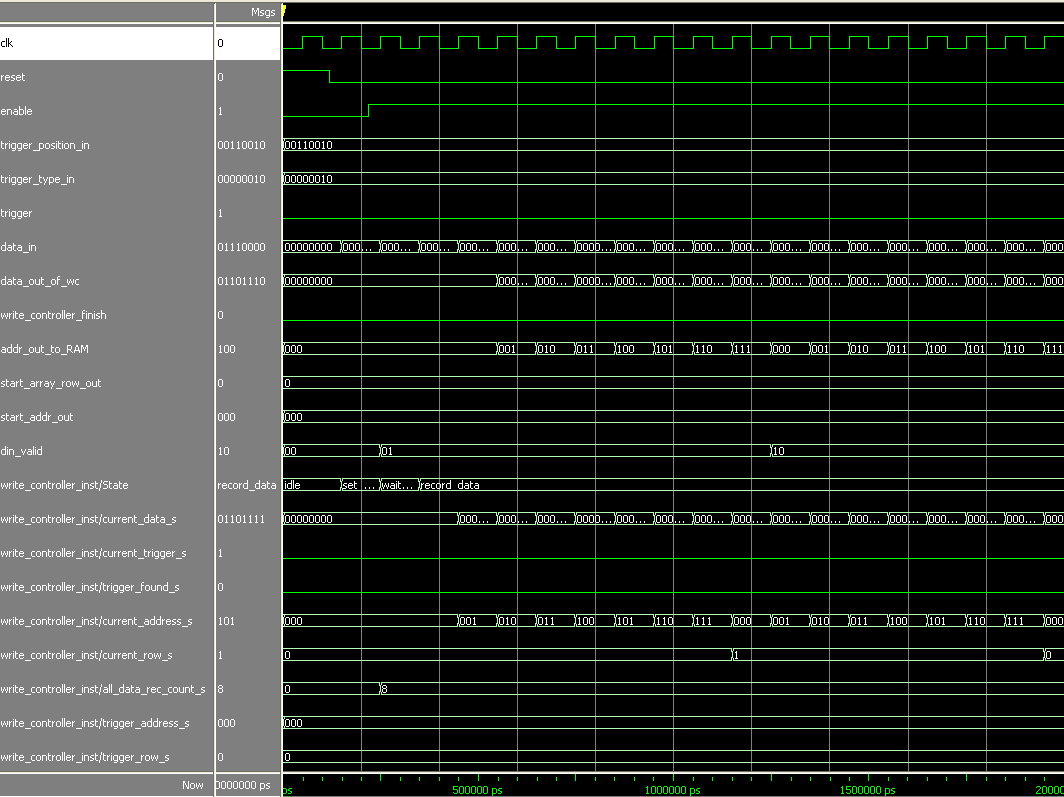
-width of a single RAM-8

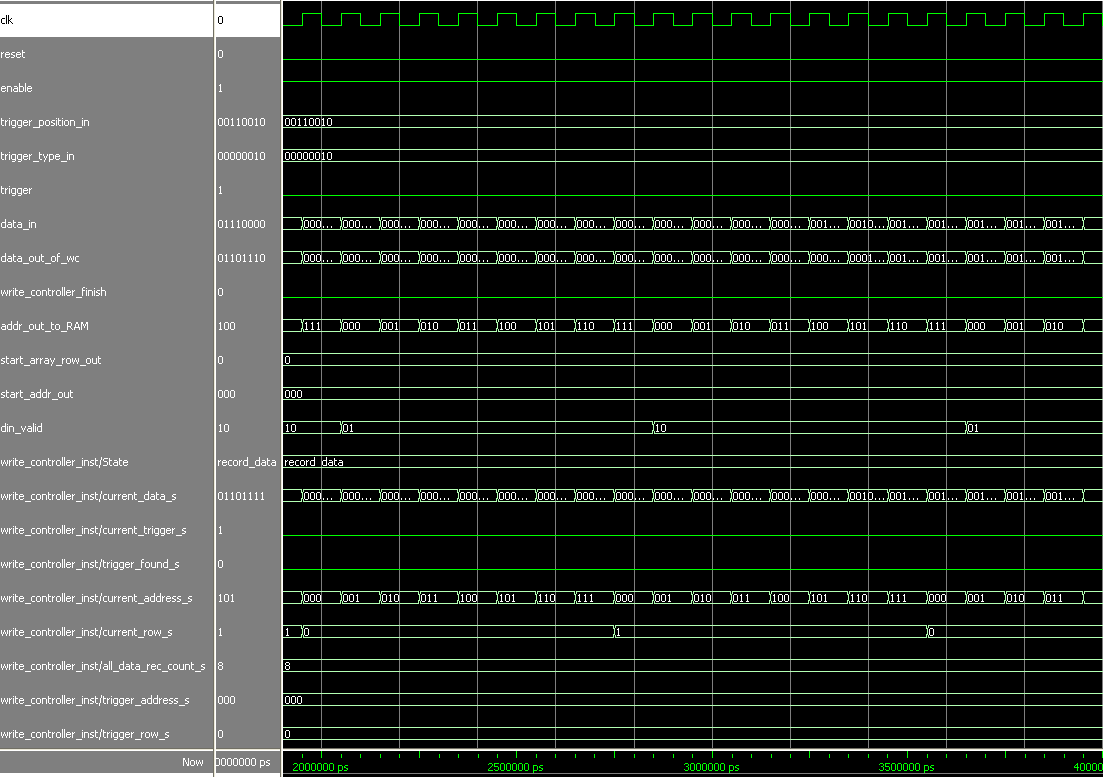
-numbers of signals for recording-8

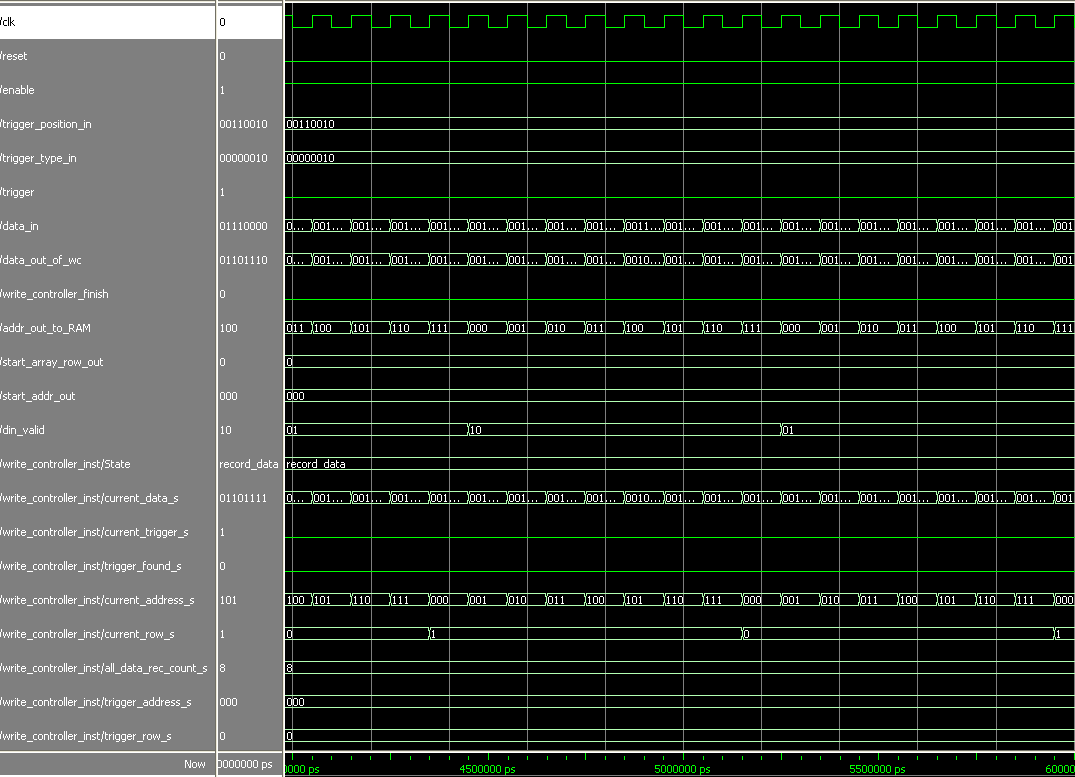
It takes two RAMs to record the entire information.

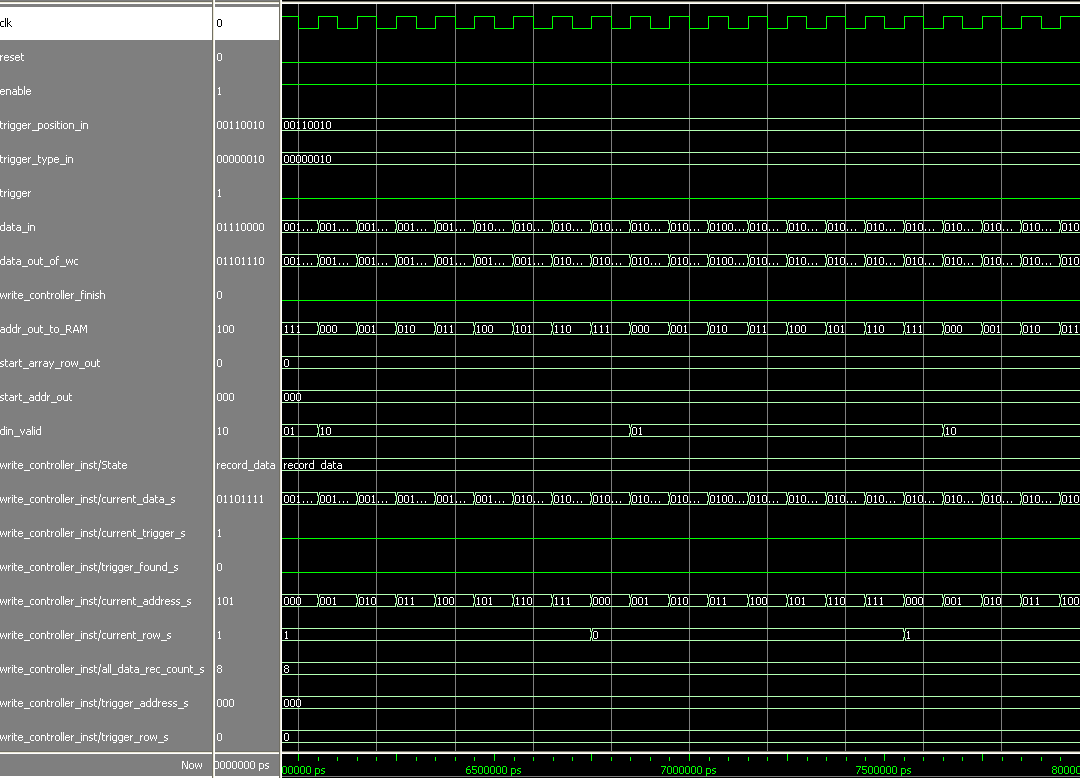
When we enable the first RAM, din\_valid=01, when we enable the second RAM, din\_valid=10. They both rise for one clock cycle in each recording cycle, the rest of the time it will be 00.

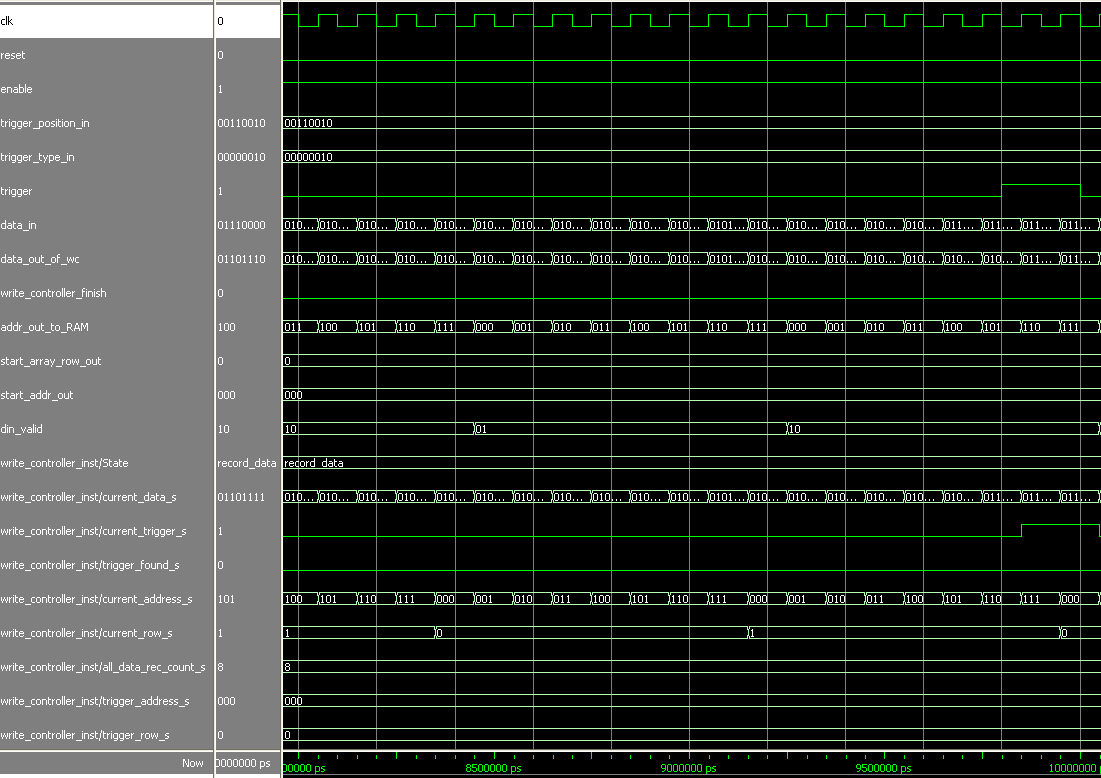
Simulation:

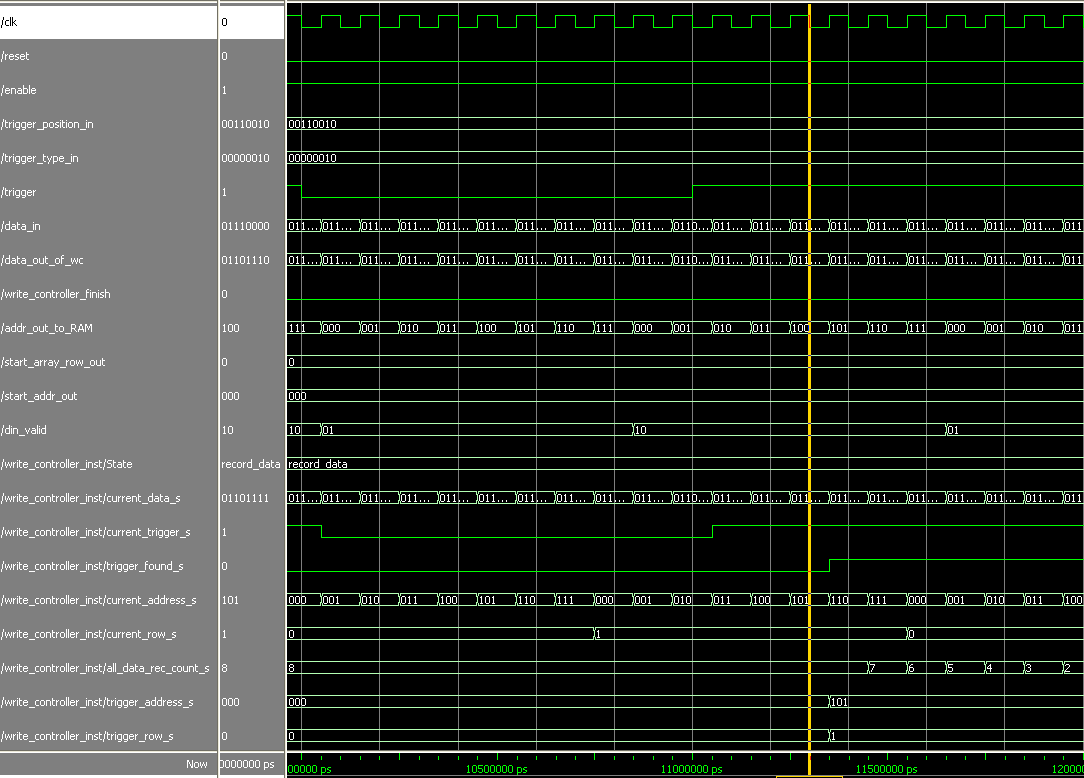


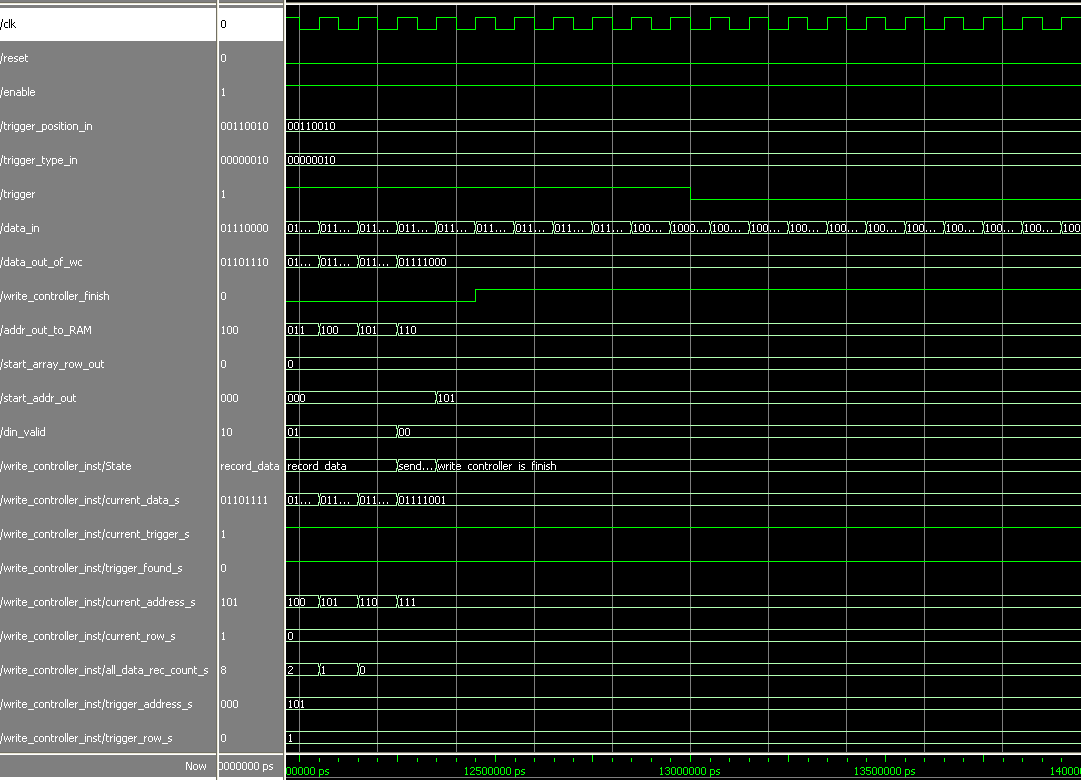


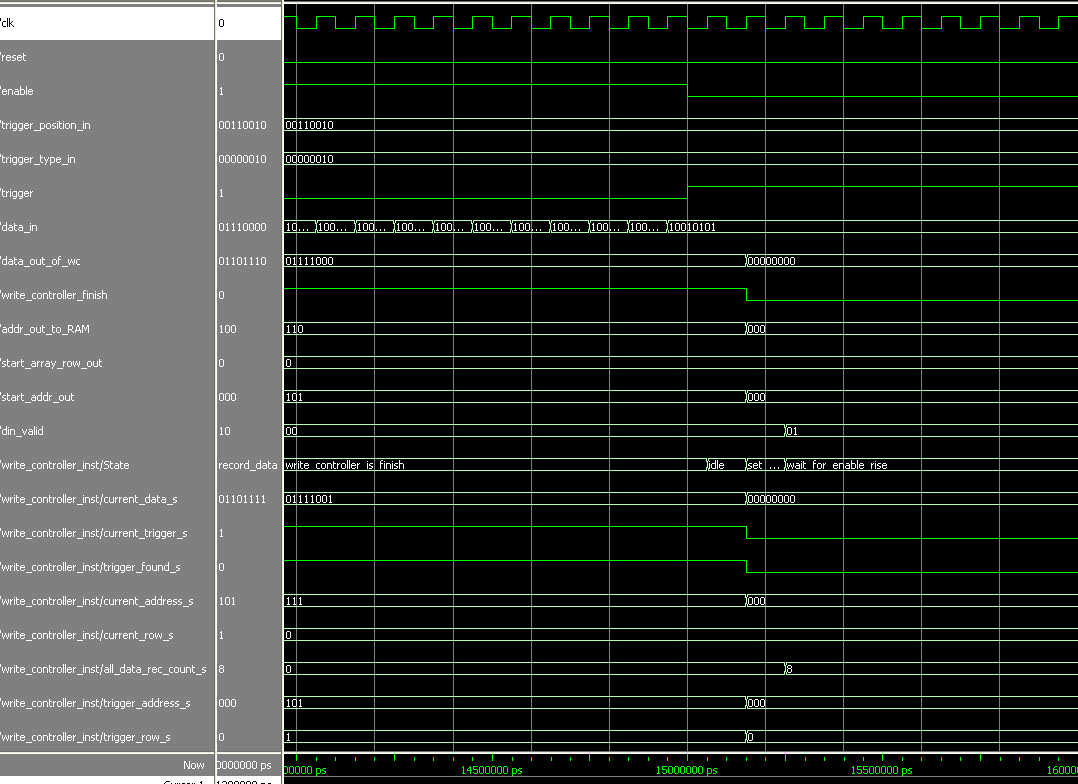


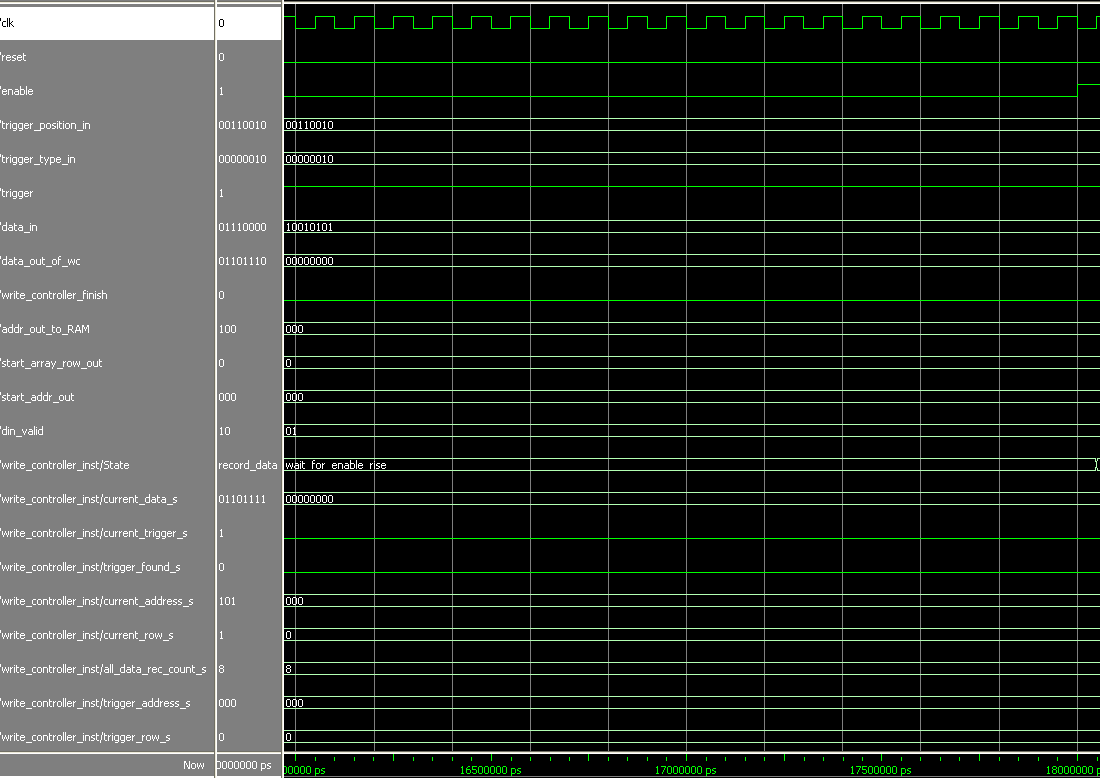


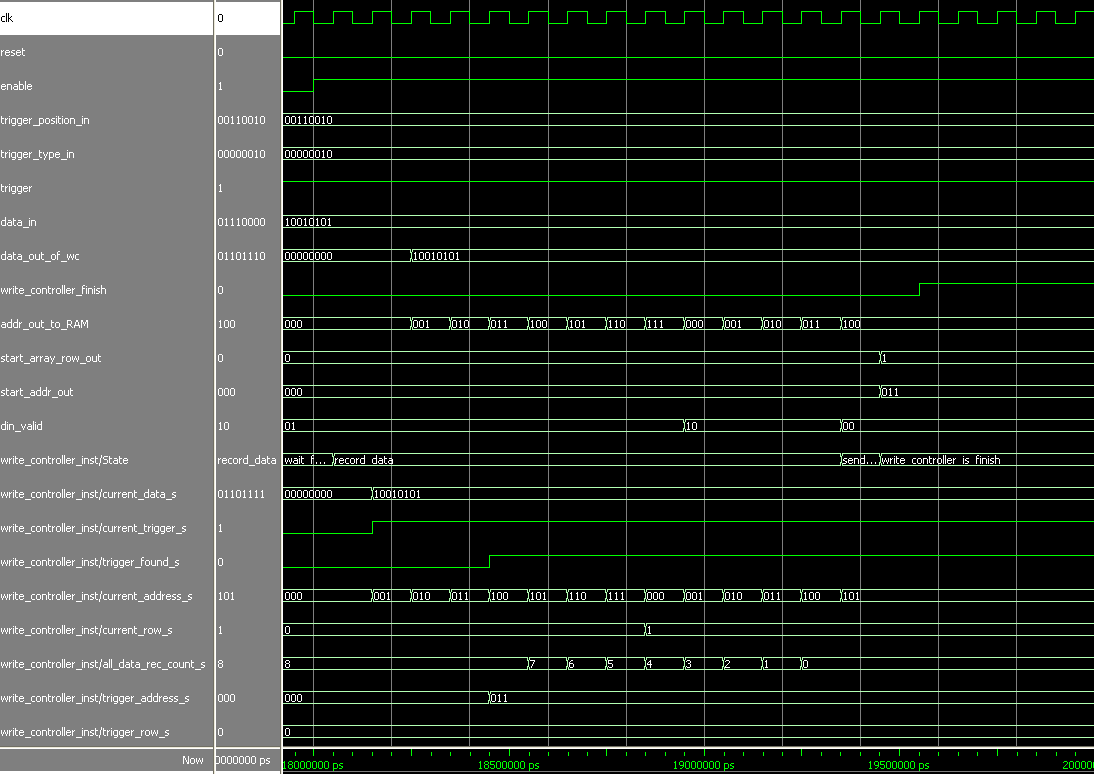












Analysis :

First we can see that trigger is rise for two cycles and the system dose not rise trigger\_found\_s, because trigger defined as 3 cycles high. After that trigger found at address 110 in row 1, because of 50% trigger position we expect that the start address will be also 110 but in the other row (row 0) and that is exactly the outcome. After we sent the start address and row the system waits for enable to fall. When that happened (15000 ns) we returns to idle mode, all signals are initialized and we start a new recording cycle.

TEST NUMBER 3

Generics values:

|  |  |  |
| --- | --- | --- |
| Comments | Value | Name |
|  | 1 | reset\_polarity\_g |
|  | 1 | enable\_polarity\_g |
| Each the number og addresses is RAM in | 3 | signal\_ram\_depth\_g |
| "word" width – line in the RAM | 8 | signal\_ram\_width\_g |
| The number of recorded signals is | 4 | record\_depth\_g |
| BUS width of the information entering the component | 8 | data\_width\_g |
| Word width in WB protocol | 8 | Add\_width\_g |
| Number of signals we record in each iteration | 8 | num\_of\_signals\_g |

Variables values:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Comments | Value | | | | Name |
| Inputs | | | | | |
|  | 50 duty cycle | | | | clk |
| Every time reset rise to 1- the system return to idle mode | 120-20000 | | 0-120 | | Reset |
| 0 | | 1 | |
|  | 220-20000 | | | 0-220 | Enable |
| 1 | | | 0 |
| 25% | 00011001 | | | | Trigger position in |
| Fall | 00000000 | | | | Trigger type in |
| Counter. Change every clk cycle | 0-150 | | | | data\_in |
|  | 10000-20000 | 0-10000 | | | trigger |
| 1 | 0 | | |
| Outputs | | | | | |
| We record a new bit every clk cycle | Update every clk cycle | | | | Data out of wc |
|  | Update every clk cycle (together with data out) | | | | addr\_out\_to\_RAM |
| 000-111 | | | |
| Rise when we recorded all the data | 11650-20000 | | 0-11650 | | write\_controller\_finish |
| 1 | | 0 | |
| When trigger is found and all data is recorded, we send out the address of the relevant data in the RAM | 11550-20000 | | 0-11550 | | start\_addr\_out |
| 101 | | 1 | |
| When trigger is found and all data is recorded, we send out the array row of the relevant data in the RAM | 11550-20000 | | 0-11550 | | start\_array\_row\_out |
| 1 | | 0 | |
| Length is number of RAMs, to enable the N RAM we put 1 in the N place and all the other is 0 | Enable the correct RAM when we send the data and address out | | | | din\_valid |
| 10 - 01 | | | |

Explanation:

The trigger type is set to 'rise'. The information will be recorded after trigger rise, meaning from the moment the trigger rises we'll wait 12 cycles (75% of 16), then we'll extract the start address to the next component.

Trigger position is 25, so we continue recording the data 75% after trigger rise.

Description of the RAM composition:

-information depth of single RAM- 8

-information depth needed for recordind-16

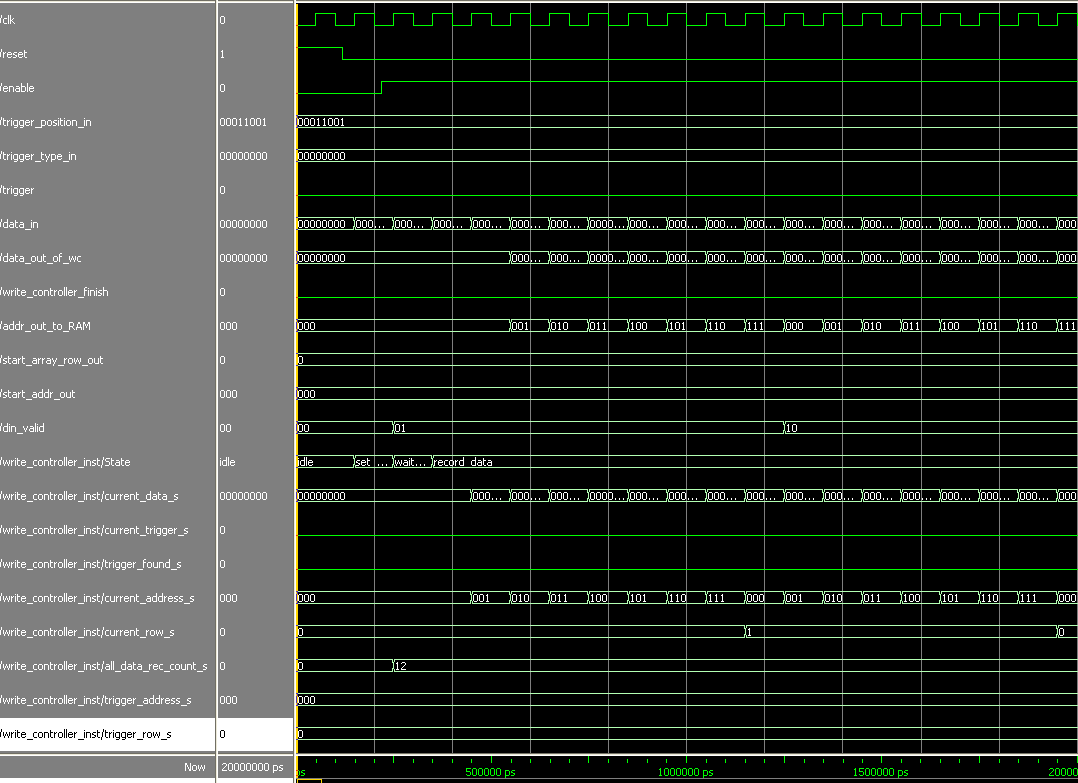
-width of a single RAM-8

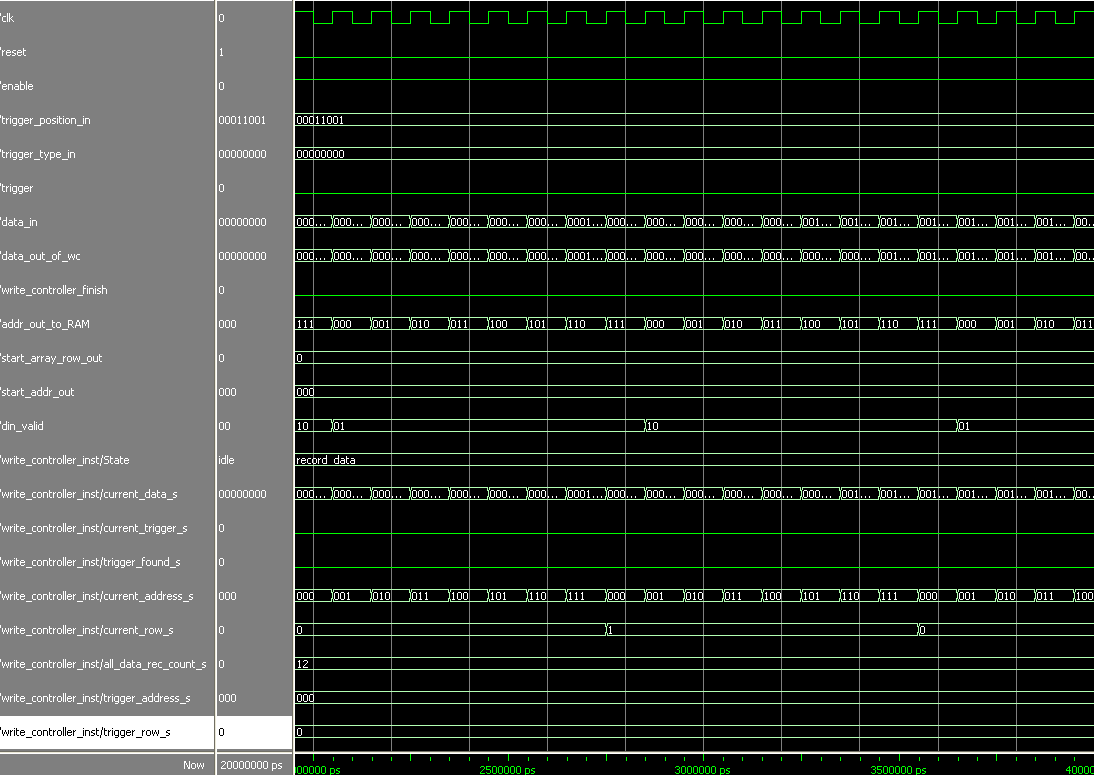
-numbers of signals for recording-8

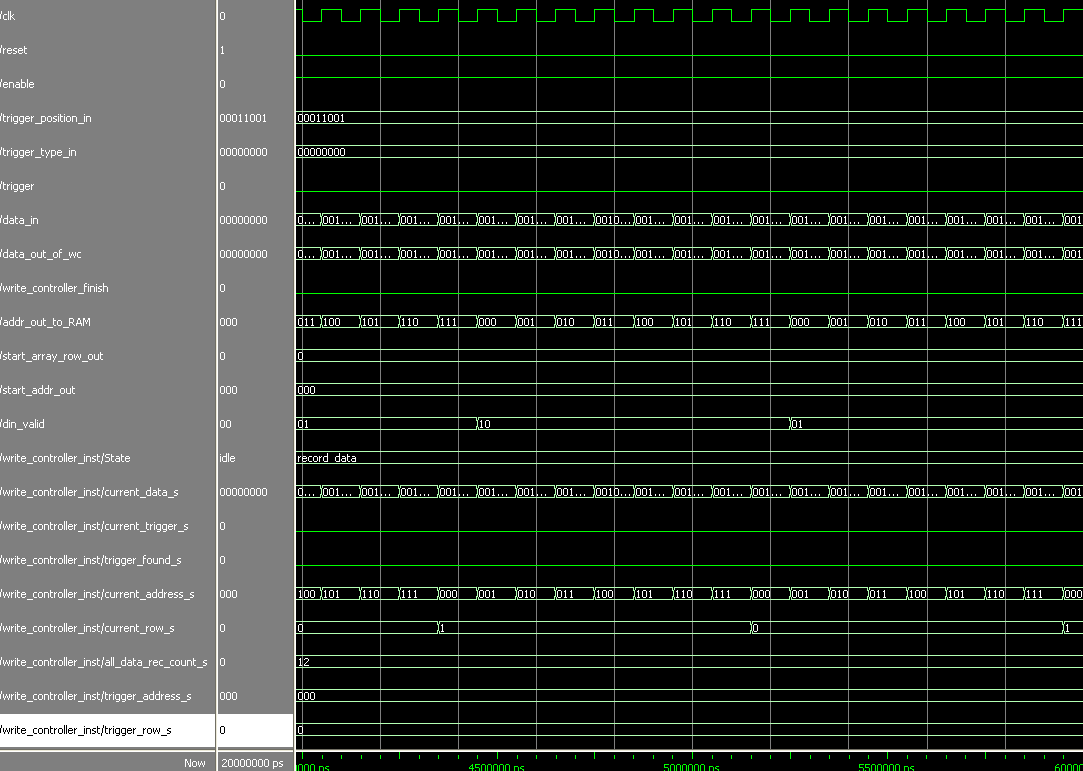
It takes two RAMs to record the entire information.

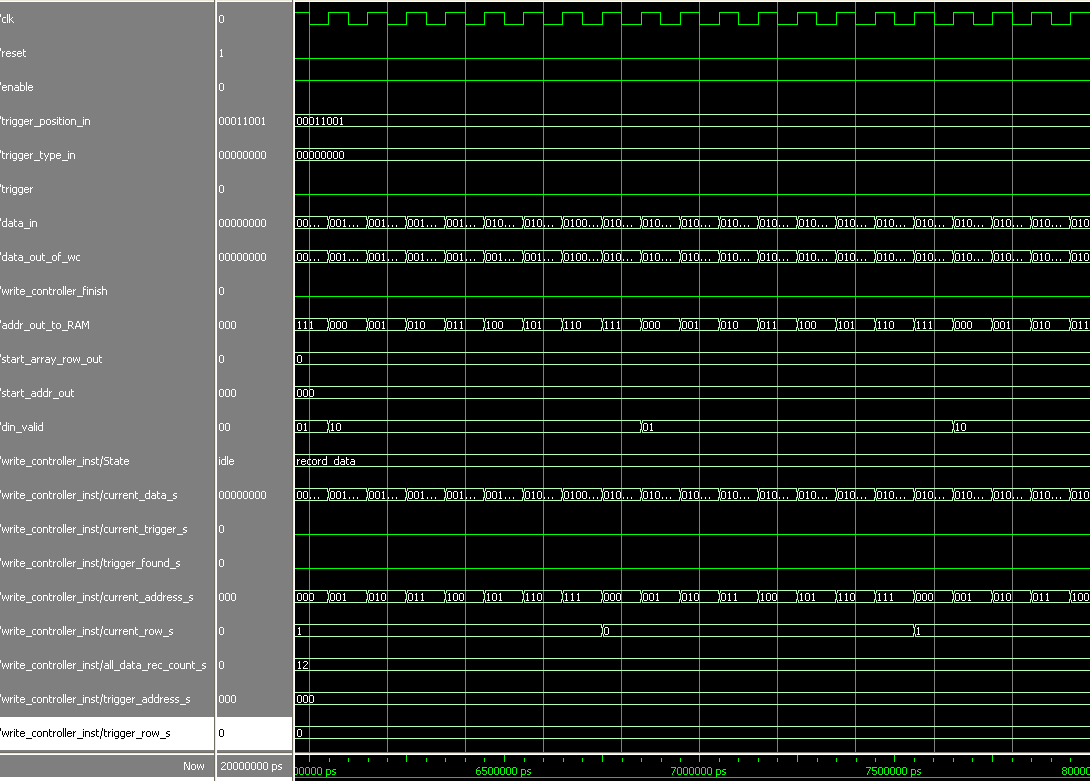
When we enable the first RAM, din\_valid=01, when we enable the second RAM, din\_valid=10. They both rise for one clock cycle in each recording cycle, the rest of the time it will be 00.

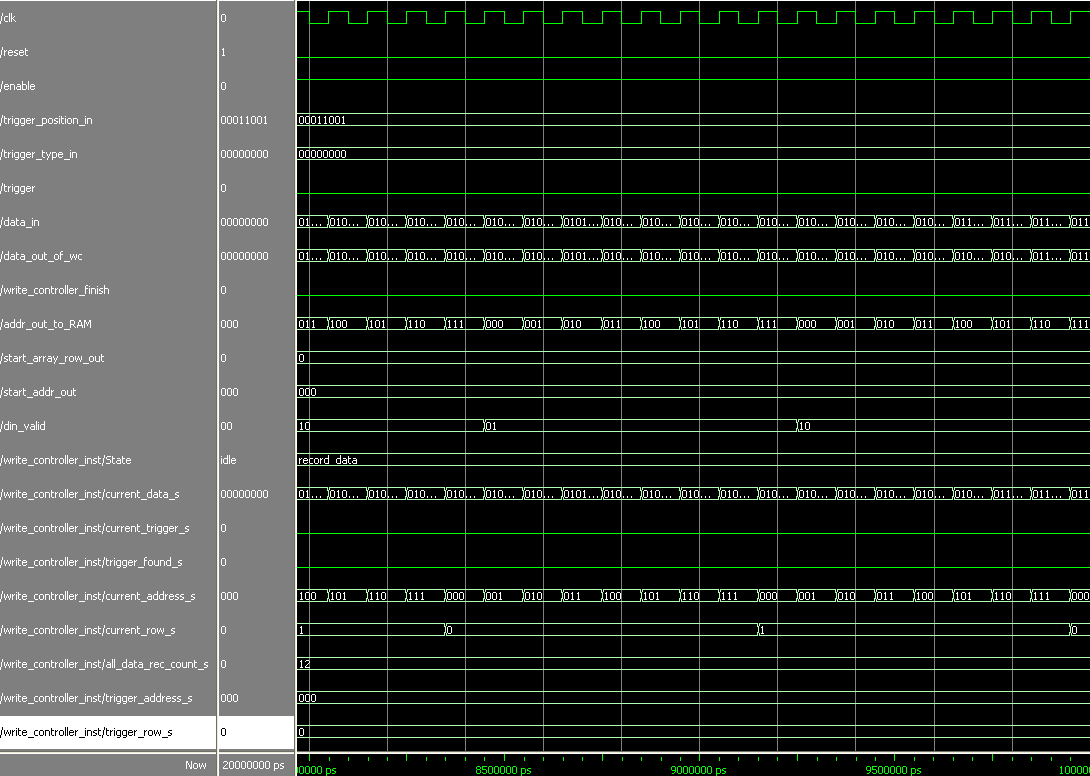
Simulation:

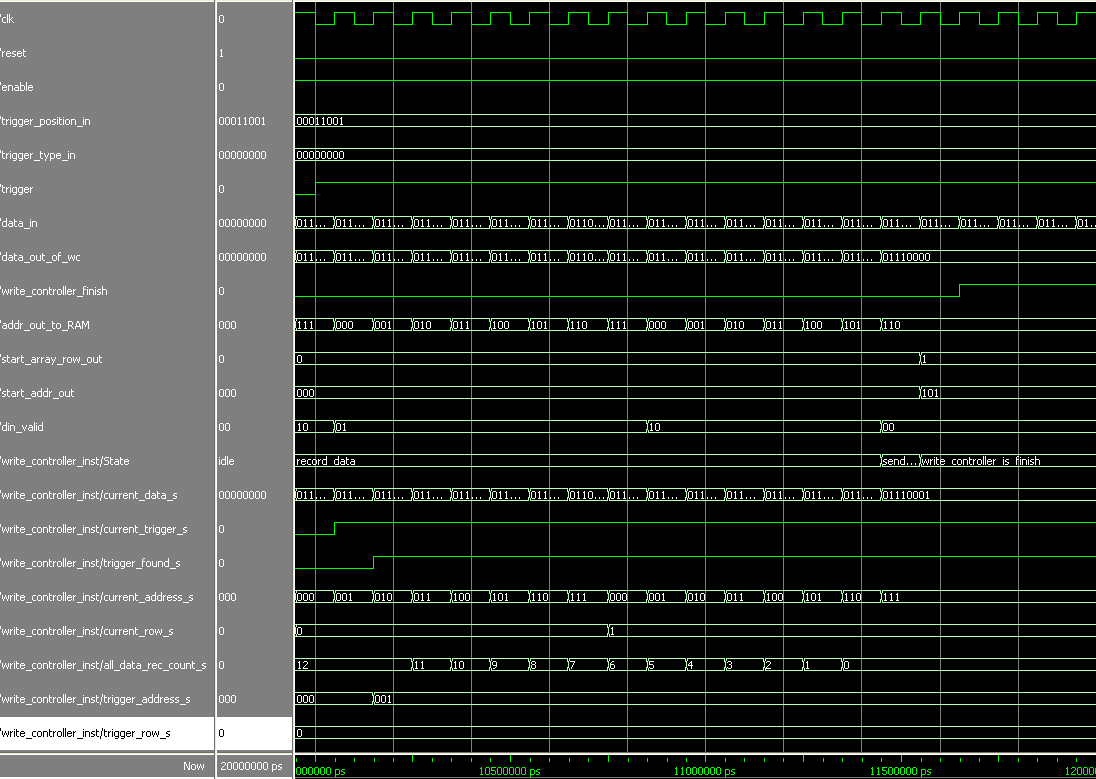












Analysis :

After trigger rise (10000 ns), the system identify that and rise trigger\_foud\_s. since that, we count 12 record cycles (trigger\_position is 25, so 75 % of recorded data will be after trigger rise) until the system finish recording the hole data. Trigger address is 001 in first RAM (row 0) and therefore the start address will be 12+1 = 13 = 8 + 5 => 101 in the second RAM.

TEST NUMBER 4

Generics values:

|  |  |  |
| --- | --- | --- |
| Comments | Value | Name |
|  | 1 | reset\_polarity\_g |
|  | 1 | enable\_polarity\_g |
| Each the number og addresses is RAM in | 3 | signal\_ram\_depth\_g |
| "word" width – line in the RAM | 8 | signal\_ram\_width\_g |
| The number of recorded signals is | 4 | record\_depth\_g |
| BUS width of the information entering the component | 8 | data\_width\_g |
| Word width in WB protocol | 8 | Add\_width\_g |
| Number of signals we record in each iteration | 8 | num\_of\_signals\_g |

Variables values:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Comments | Value | | | | | | | | | Name |
| Inputs | | | | | | | | | | |
|  | 50 duty cycle | | | | | | | | | clk |
| Every time reset rise to 1- the system return to idle mode | 600-20000 | | 430-600 | | 120-430 | | | 0-120 | | Reset |
| 0 | | 1 | | 0 | | | 1 | |
|  | 220-20000 | | | | | 0-220 | | | | Enable |
| 1 | | | | | 0 | | | |
| 50% | 00110010 | | | | | | | | | Trigger position in |
| Fall | 00000001 | | | | | | | | | Trigger type in |
| Counter. Change every clk cycle | 0-150 | | | | | | | | | data\_in |
|  | 15000-20000 | 13000-15000 | | 11000-13000 | 10000-11000 | | 1300-10000 | | 0-1300 | trigger |
| 1 | 0 | | 1 | 0 | | 1 | | 0 |
| Outputs | | | | | | | | | | |
| We record a new bit every clk cycle | Update every clk cycle | | | | | | | | | Data out of wc |
|  | Update every clk cycle (together with data out) | | | | | | | | | addr\_out\_to\_RAM |
| 000 - 111 | | | | | | | | |
| Rise when we recorded all the data | 11250-20000 | | | | 0-11250 | | | | | write\_controller\_finish |
| 1 | | | | 0 | | | | |
| When trigger is found and all data is recorded, we send out the address of the relevant data in the RAM | 11400-20000 | | | | 0-11400 | | | | | start\_addr\_out |
| 100 | | | | 0 | | | | |
| When trigger is found and all data is recorded, we send out the array row of the relevant data in the RAM | 11400-20000 | | | | 0-11400 | | | | | start\_array\_row\_out |
| 0 | | | | 0 | | | | |
| Length is number of RAMs, to enable the N RAM we put 1 in the N place and all the other is 0 | Enable the correct RAM when we send the data and address out | | | | | | | | | din\_valid |
| 10 - 01 | | | | | | | | |

Explanation:

The trigger type is set to be fall. Half of the information will be recorded after trigger fall, and half before that. From the moment that we find trigger fall we'll wait 8 clock cycles, then we'll extract a start address to the next component.

Description of the RAM composition:

-information depth of single RAM- 8

-information depth needed for recordind-16

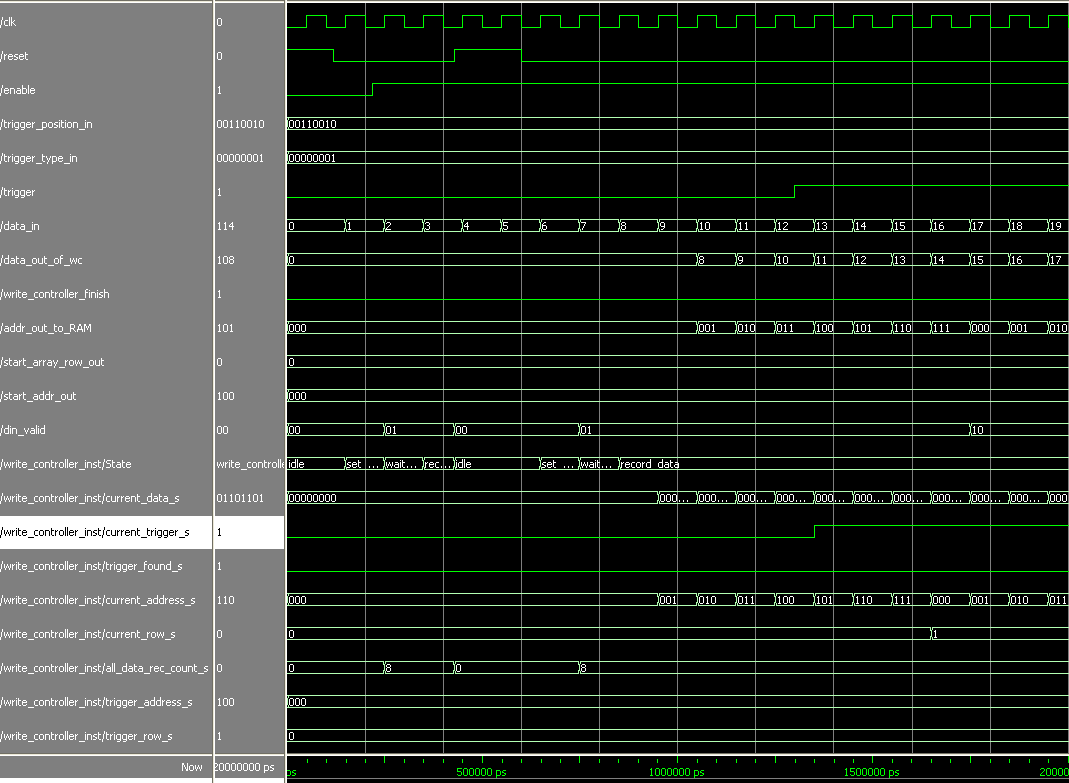
-width of a single RAM-8

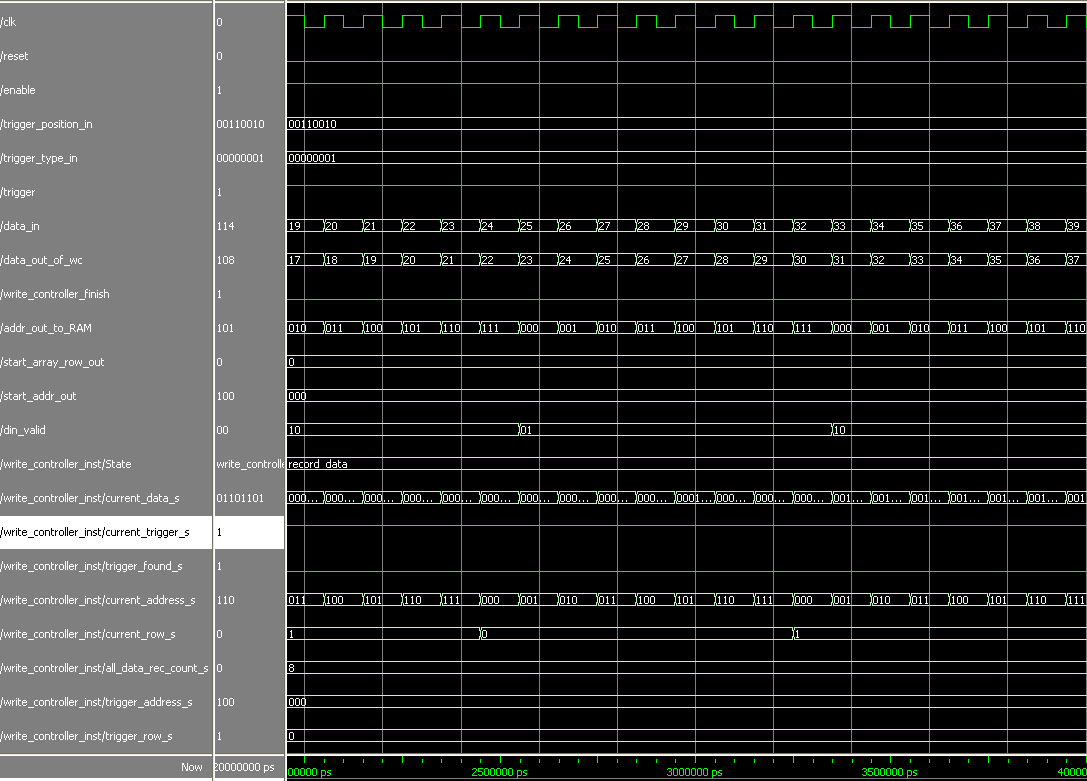
-numbers of signals for recording-8

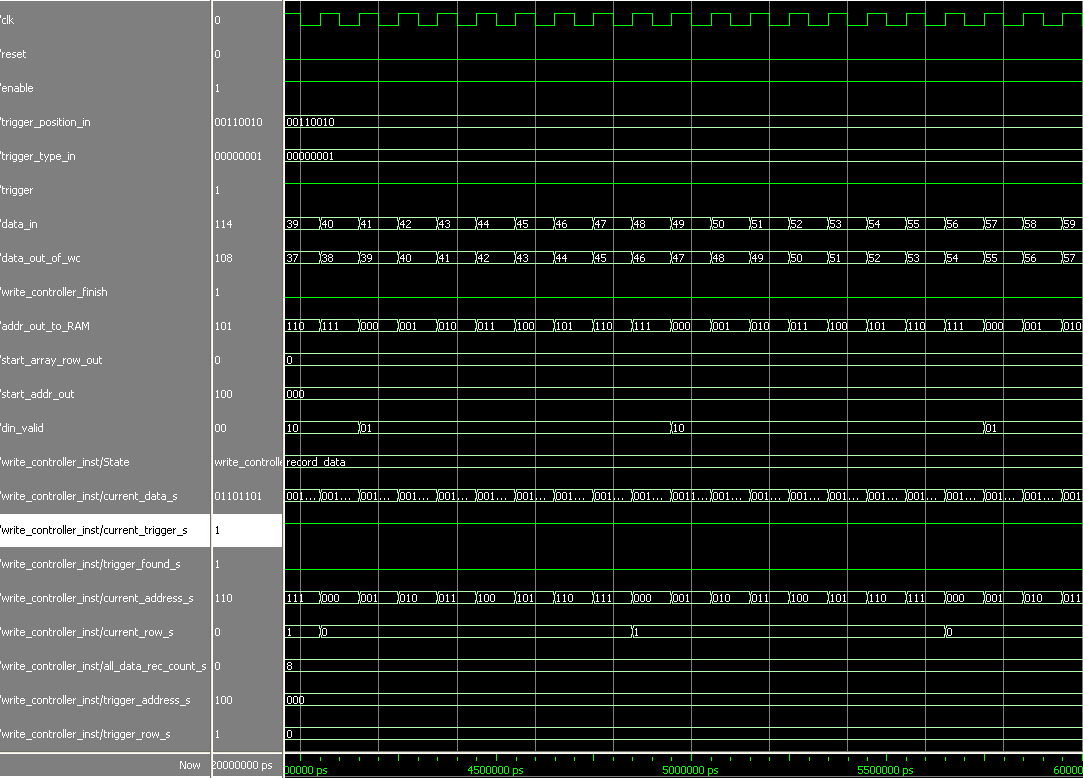
It takes two RAMs to record the entire information.

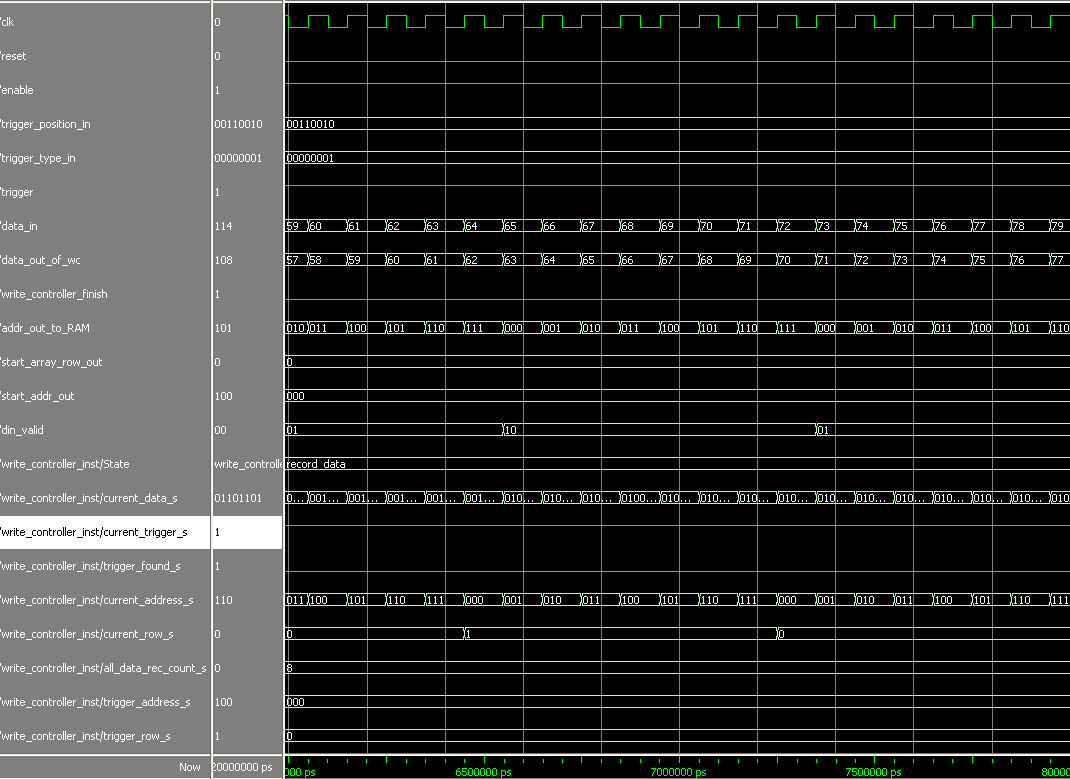
When we enable the first RAM, din\_valid=01, when we enable the second RAM, din\_valid=10. They both rise for one clock cycle in each recording cycle, the rest of the time it will be 00.

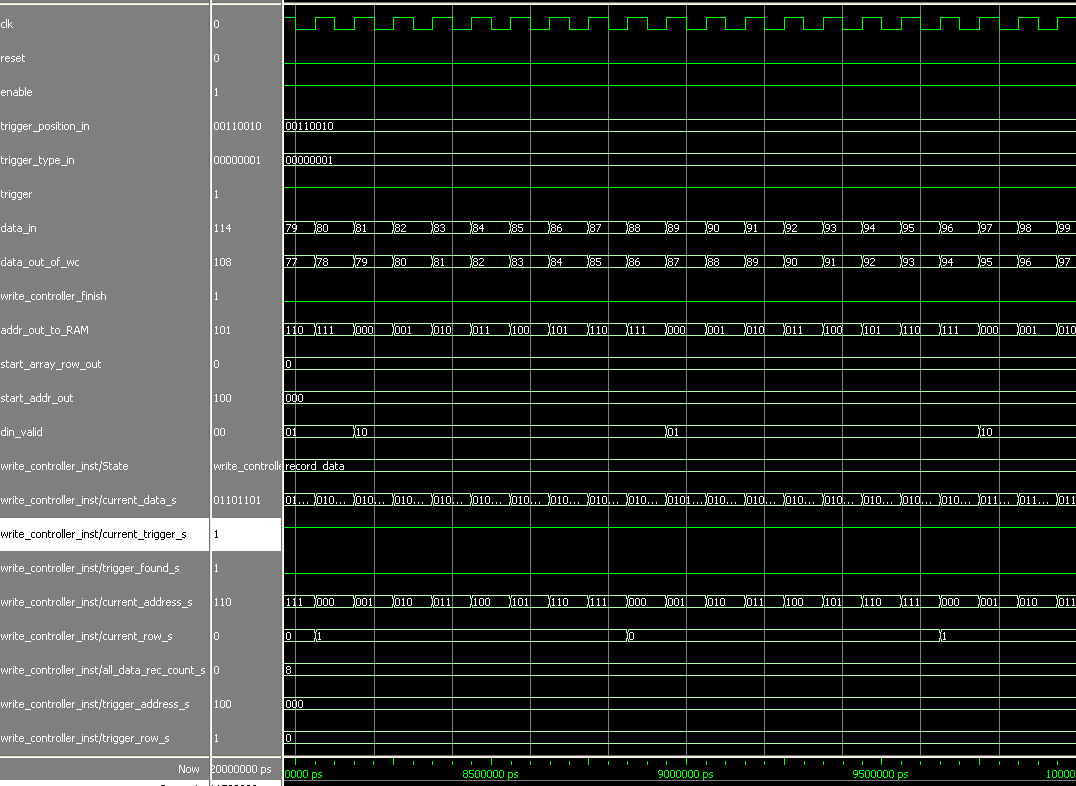
Simulation:

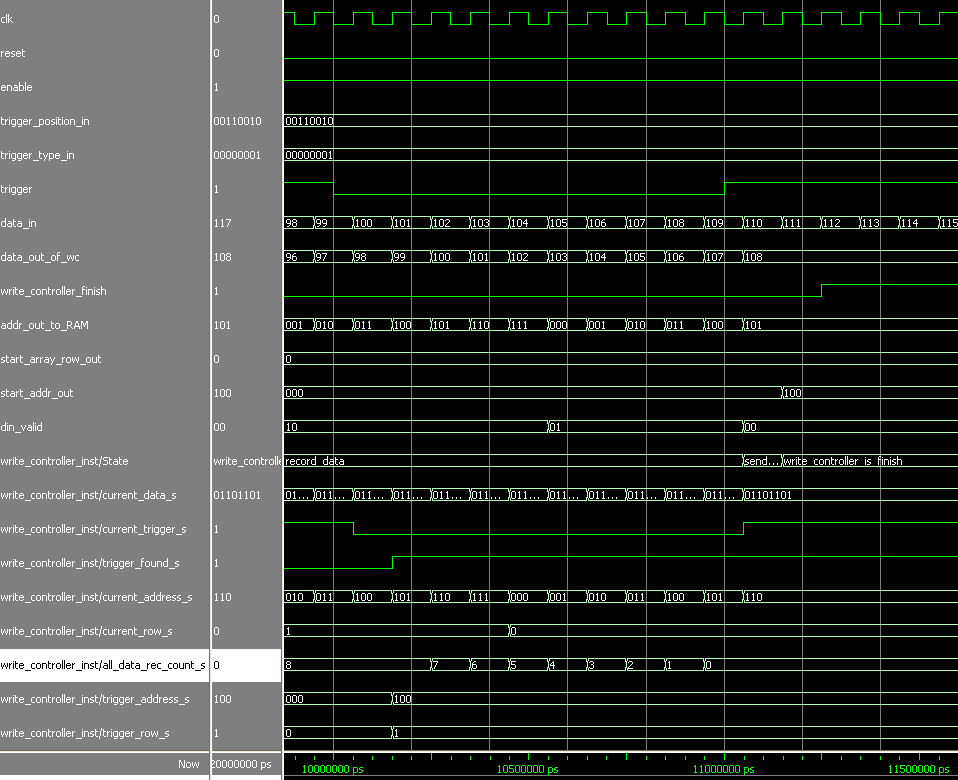












Analysis :

At first trigger is low, but we not detect trigger rise, because we search for trigger fall. After that reset is rise again and we can see that the system is returns to IDLE mode. Next trigger is fall and then we detect the trigger. Trigger is rise and fall again after that but the system is staying with the initial trigger fall. Trigger is sampled in address 100 at row 1, and trigger position is 50%, so the start address is also 100 in the row 0.

We can also see that every clk cycle we sample the incoming data, calculating a new address and send them both to the RAM.